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(54) Title: MULTIPLE–SOURCE TRANSMISSION SYSTEM

(57) Abstract

An advertisement insertion system arranged to substitute a local advertisement in place of a national advertisement arriving over a national television feed signal for community television. The system includes a compressed digital source for storing the local advertisement as well as a signal processor which has as inputs both the national television feed signal and the digital source. The national television signal includes a standard television signal and a cue tone which is used to select the data from the digital source for delivery to the signal processor. The signal processor generates a timing signal from the vertical synchronization signal of the standard television signal, and also converts the selected data to an alternative television signal synchronized to the national television signal. The signal transmitted by the signal processor, in response to the cue tone, is either the national television signal or the alternative television signal. The signal processor controls the flow of data from the digital source so the selected data is available to reconstruct the alternative television signal as needed.

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MULTIPLE-SOURCE TRANSMISSION SYSTEM

FIELD OF THE INVENTION

This invention relates generally to subscriber systems, such as community antennae television (CATV) systems, for processing and delivery of video, audio, and data services and, more particularly, to circuitry and a concomitant methodology for selectively delivering the services from multiple sources.

BACKGROUND OF THE INVENTION

Conventional subscriber systems, such as cable television systems, are typically arranged to provide viewer programs according to a pre-determined time schedule. The programs available to the subscribers of a particular system are most often provided by a national network source and transmitted to the headend of a given local system over, for instance, a satellite link. An integrated receiver-detector (IRD) located at the headend provides the video, audio, and cue tone signals for each national network source. The national network programmers provide certain intervals -- designated breaks -- during each program for use by the local cable programmer. For instance, it is common to set aside approximately four minutes in each half-hour for local insertion of commercial advertisements (ad-insertion) particularly relevant to the local subscribers of the given

system. The time of occurrence of each break is generally indicated by the cue tone signal delivered as part of the national network feed signal. Accordingly, it is necessary to provide the local cable programmer with the capability of alternately selecting multiple sources of program information to thereby substitute local advertisements in place of national advertisements, in consonance with the cue tone indications, at the discretion of the local programmer.

One conventional technique for ad-insertion is characterized by a combination of a cue tone detector, controller, switching equipment for both video and audio, and tape players which hold the local advertising material. The different cue tones that may be transmitted in the television program feed include: (1) a pre-roll period (to allow the videotape player to attain operating speed; (2) a transfer-to-ad signal (the beginning of the advertisement transmission interval); and (3) a return signal (to return to the transmission from the national network source). The cue tones have the format of standard dual-tone multi-frequency (DTMF) signals.

In one typical operational sequence, the series of cue tones detected by the cue tone detector serve as inputs to the controller. The controller activates a local tape player, which has a mounted tape containing the desired advertisement, in response to the pre-roll cue tone. The switching equipment, when notified by the controller of the

transfer-to-ad cue tone, then switches the subscriber system from the incoming national video and audio signals to the output of the local tape player for the duration of the advertisement. Finally, the switching equipment returns the subscriber system to the incoming national network feed upon receipt of the return cue tone.

In another possible operational sequence, only the pre-roll cue tone may be required. In this scenario, the local cable programmer knows that for the given cable channel the pre-roll time is a fixed time duration; immediately following this interval, the switch to the local advertisement is effected. It is also known to the local programmer that each break is of a fixed duration, so switching back to the national feed will occur after this fixed duration. Thus, only the pre-roll cue tone is utilized during this operational sequence; the transfer-to-ad and return cue tones need not be sent, or if they are sent, may be ignored (or used for error checking if desired).

A necessary feature of any ad-insertion system, as is true in any multiple-source transmission system, is ability to synchronize the local or secondary source of information (e.g., the output of the tape player) with the primary signal (e.g., the national-feed television signal). If the secondary source is not synchronized to the primary signal when the switching equipment operates, vertical roll

or undesired noise may occur. Modern ad-insertion systems include synchronization circuitry as part of the controller or switching equipment to supply horizontal and vertical synchronizing signals to enable the secondary signal derived from the secondary source to be synchronized with the primary signal prior to switching to and from the secondary source.

Because of the well-known benefits of digital storage and high-speed digital transmission, including such benefits as more efficient use of bandwidth, inherent reliability, and error-correction capability, many existing analog storage and delivery systems are undergoing conversion to digital systems. Ad-insertion systems are currently being developed wherein a digital data source such as a digital file server or memory replaces the video tape player of the conventional analog systems. The digital source stores the commercial advertisement data in digital form, rather than analog, in low-cost, high capacity digital storage media, such as hard disks. In order to optimize use of the digital storage, the commercial advertisement data most often is compressed according to a data compression algorithm, such as an MPEG (Moving Picture Experts Group) algorithm. When insertion of a commercial advertisement stored in the digital source is desired, the particular advertisement of interest must be located in local storage, retrieved, decompressed, and converted to an analog signal for transmission over the cable television distribution

system. Because of the additional steps involved in inserting an advertisement stored in compressed digital format in a data source, the problem of synchronizing the commercial advertisement to the analog cable television signal is exacerbated.

Moreover, although the MPEG-compressed data stream representative of the commercial advertisement includes timing information, such information is generally not useful for proper synchronization between the ad-insertion signals and the national television programming signals because the signals are supplied from different sources. In effect, the timing information in the MPEG stream is irrelevant with respect to the national program signal. Accordingly, there is a need for processing circuitry for synchronizing the secondary MPEG source to the primary source (in the terminology of ad-insertion, synchronizing the local digital source to the national analog source), and for switching the cable transmission to and from the separate analog and digital sources.

In addition, in any real-time system utilizing a digital source to derive an analog signal, there is a need to provide the requisite number of data bits in a timely manner so that analog signal may be generated and transmitted to preserve the real-time characteristics of the system. In the current digital art, each channel is derived from a single storage medium and a concomitant storage

controller. In a system wherein there are mismatches in capacity between the digital source and the analog generation circuitry, such as will occur when digital data must be retrieved from local storage and transmitted as a digital stream over a transport medium, the real-time operation is aided by the use of intermediate buffer memory. The buffer memory ensures the requisite bits are available when needed. The proper sizing of the buffer memory, and even the possible deployment of multiple intermediate buffer memories, are important design parameters. Too little memory will cause lost analog frames, and too much memory is costly. A so-called back-flow control mechanism, operating to control the flow of data from the digital source in response to control signals emitted by the analog generation circuitry, can optimize the sizing and location of buffer memory. Thus, there is a need for circuitry for ensuring that the digital source provides the digital data in a controlled manner so that no analog frames are dropped nor are analog frames repeated due to either overflow or underflow of the rate of delivery of a digital data stream from the digital source to the processing circuitry.

Normally, in a system utilizing MPEG data streams, the operational mechanism is one wherein the MPEG digital source is the master of downstream circuitry, that is, the downstream circuitry must be arranged to process the incoming data bits without any ability to control the rate at which incoming bits arrive. The back-flow control

mechanism described above is essentially the converse of the normal MPEG operation in that the digital source is controlled by the analog generation circuitry, that is, the flow of the MPEG compliant data stream is controlled by autonomous circuitry external the source of the MPEG streams.

SUMMARY OF THE INVENTION

These shortcomings and other deficiencies and limitations are obviated, in accordance with the present invention, by a system in which an output signal is alternately produced from either a primary signal or a secondary signal derived from a data source in correspondence to a control signal conveyed with the primary signal, and wherein the primary and secondary signals are synchronized upon transfer from one signal to the other signal.

Broadly, the system includes circuitry to: (1) generate a timing signal from the primary signal; (2) convert a data stream obtained from the data source, based on the control signal, to the secondary signal synchronized to the timing signal; (3) control the flow of the data stream from the data source; and (4) switch between the primary signal and the secondary signal in response to the control signal.

In a preferred embodiment of the broad aspect of the present invention, the system for delivering an output signal corresponding to a primary source in one interval and representative of an autonomous signal source in another interval is a signal processor having a national network feed television signal as the primary source, and a digital data source as the autonomous signal source. The national video feed then includes a conventional television signal and at least one cue tone indicating an interval for which the output signal corresponds to the digital data source. The signal processor includes a channel interface controller which is coupled to the video source; the channel interface controller ultimately emits the output signal. In addition, the signal processor includes a system interface controller interposed between the digital data source and the channel interface controller. The system interface controller stores a data stream provided by the digital data source as stored data for the channel interface controller. The channel interface controller is arranged with the following functionality: (a) generation of a timing signal from the national network feed signal -- in particular, the timing signal is indicative of the vertical synchronization signal; (b) receiving and storing the stored data as transmitted from the system interface controller; (c) conversion of the stored data to an alternative television signal synchronized to the timing signal; and (d) selection of either the television signal or the alternative television signal as the output signal in correspondence to the cue tone.

Moreover, the system interface controller is arranged to control the flow of the data stream propagated by the digital data source in response to flow control information passed from the channel interface controller to the system interface controller.

These and other aspects and features of the invention will be more clearly understood and better described when the following detailed description is read in conjunction with the attached drawings, wherein:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a high-level block diagram of the system processor, including a system interface controller and a channel interface controller, in accordance with the present invention;

FIG. 2 is a block diagram depicting certain circuit blocks of FIG. 1 in more detail;

FIG. 3 depicts a block diagram of the video data and signal flow control portion of the block diagram of FIG. 2 in more detail;

FIG. 4 depicts a block diagram of the audio data and signal flow control portion of the block diagram of FIG. 2 in more detail;

FIGS. 5 and 6 depict the detailed physical structure of an illustrative compressed data bus and an illustrative control bus, respectively, coupling the channel interface controllers to the system interface bus;

FIG. 7 is a diagram of pertinent elements for controlling the flow (back-flow control) of data to a given channel interface controller from the system interface controller;

FIG. 8 is a diagram of pertinent elements for controlling the flow (back-flow control) of data to the system interface controller from the signal source;

FIG. 9 is a diagram of pertinent elements for interrupt processing as initiated by a given channel interface controller;

FIG. 10 is a high-level state diagram of the processor tasks for the signal processor in accordance with the present invention;

FIGS. 11-14 depict a flow diagram representing the major processing steps in generating the analog video and audio from the signal source for substitution into the national video feed;

FIG. 15 is a high-level state diagram of the processor tasks for the transfer processor in accordance with the present invention;

FIG. 16 is a high-level state diagram of the processor tasks for the system processor in accordance with the present invention; and

FIG. 17 is a high-level state diagram of the processor tasks for the channel processor in accordance with the present invention.

In the figures, the same reference numeral is used to identify the same element which may appear in multiple figures.

DETAILED DESCRIPTION

To fully appreciate the import of the signal processing system of the present invention as well as to gain an appreciation for the underlying operational principles of the present invention, it is instructive to first present, in overview manner, a high-level description of the overall system. This overview also serves to introduce terminology so as to facilitate the more detailed description of building-block components of the signal processing system which follows the overview presentation.

Overview of the Signal Processing System

With reference to FIG. 1, there is shown signal processor 100 in accordance with an illustrative embodiment of the present invention. Broadly, processor 100 receives as inputs: (a) compressed digital information, representative of the advertisements to be inserted during breaks in national programs, in MPEG-2 compliant format from signal source 150 over source bus 101; and (b) analog video signals from network video source 160 over one or more channel inputs 102, 103, ..., 104. Outputs from processor 100, in correspondence to the number of channel inputs, are provided to one or more modulators 170, 171, ..., 172 over channel outputs 105, 106, ..., 107, respectively. The modulators also have as an input modulator bus 108 emanating from processor 100; the carrier frequency of each modulator is controlled by processor 100 over modulator bus 108. Accordingly, each modulator delivers a single, narrow-band analog signal serving as one of the numerous input channels to the broadband signal spectrum offered by the local cable programmer. The outputs from each of the modulators are combined in a radio frequency (RF) channel combiner 180 to generate the broadband offering of a particular CATV service; the output of combiner 180 appears on transmission output 109.

In particular, processor 100 receives digital information in a data stream from signal at least one

source 150 and, in the case of NTSC, converts the data stream into one analog video and two analog stereo audio signals per channel. Processor 100 also receives one analog video and audio input from video source 160 over each channel input 102 , 103, ..., 104 as the network feed; each channel input may, for example, be derived from a conventional IRD (integrated receiver-detector) device responsive to a national video feed signal detected over a satellite link. Each channel input also has a time-ordered series of conventional cue tones at intervals controlled by the programmer of video source 160 as indicators for ad-insertion. As guided by the incoming cue tones on a given channel input (say 102), the outgoing signal on the corresponding channel output (105) is either the television signal provided by the given channel input (102) or, alternatively, the video (e.g., NTSC) signal derived from signal source 150.

Processor 100 is composed of system interface controller 110 and one or more channel interface controllers 130, 131, ..., 132, each coupled to system interface controller 110 via channel bus 111. In one preferred embodiment, there are eight channel interface controllers (i.e., N=8 in FIG. 1). Source bus 101 couples signal source 150 to system interface controller 110. Channel interface controller 130 receives as input the signal from video source 160 appearing on input 102, and the output from channel interface controller 130 is the channel

output 105 coupled to modulator 170. Similarly, channel interface controller 131 receives as input the signal appearing on input 103, and the output of channel interface controller 131 provides the channel output 106 to modulator 171. Modulator bus 108 is connected to system controller 110.

In operation, system interface controller 110 communicates with signal source 150 over two separate logical-type interfaces, namely, a data connection and a control connection. With respect the data connection, system interface controller 110 receives MPEG-2 transport packets from signal source 150 through, illustratively, a SCSI-2 Fast and Wide Interface, that is, source bus 101 includes a parallel bus that supports the SCSI-2 Fast and Wide standard protocol. During data transfers, a data stream of MPEG-2 transport packets, representing a subset of data available from signal source 150, is received by system interface controller 110. The incoming packets are routed under control of system interface controller 110 into a plurality of program files (i.e., different areas of memory) and stored in such different areas of memory in correspondence to the number of channel interface controllers (130, 131, ..., 132), and are stored by system interface controller 110. A program file is composed of MPEG-2 standard transport streams encapsulating related elementary streams such as audio, video, and control. In broad terms, system interface controller 110 receives the

program files as a number of SCSI-2 logical devices, again in correspondence to the number of channel interface controllers, even though there may be only one physical interface. With respect to the control connection, controller 110 and source 150 communicate using, illustratively, an Ethernet link; thus source bus 101 also is composed of this separate Ethernet link. The protocol used over the Ethernet link is the standard TCP/IP protocol.

System interface controller 110 communicates with each channel interface controller 130, 131, ..., 132 via channel bus 111, which is also partitioned into two separate logical interfaces, namely, a data connection and a control connection. The data connection supports high-bandwidth data transfer in essentially a unidirectional manner from system interface controller 110 to each channel interface controller 130, 131, ..., 132. The control connection is a low band-width link which carries both control and status information. Both logical connections of bus 111 use specially designed protocols to maximize the flow of data and control between system interface controller 110 and each channel interface controller 130, 131, ..., 132. As guided by ad-insertion control signals communicated over bus 111, system interface controller 110 supplies the stored MPEG-2 transport streams over bus 111 to each channel interface controller 130, 131, ..., 132, wherein the MPEG-2 transport streams are parsed into MPEG elementary data streams for conversion to a composite NTSC signal. The composite NTSC

signal is representative of a given advertisement stored originally as digital data. Prior to substitution of the advertisement into the appropriate interval of each channel output indicated by a detected cue tone, the composite NTSC signal is synchronized with the incoming national feed signal from video source 160, and then switching from video source 160 to the composite NTSC signal is effected in correspondence to the cue tone information.

In the delivery of MPEG-2 digital data from signal source 150 to system interface controller 110 and, in turn, to channel interface controllers 130, 131, ..., 132, timing conventionally derived from the MPEG-2 transport stream is replaced by timing derived from the video source 160. Thus, prior to switching from the primary signal delivered by video source 160 to the secondary signal derived from signal source 150, it is necessary to exert back-flow control to decrease the rate or even temporarily inhibit the delivery of MPEG-2 data to one or more of the controllers 130, 131, ..., 132. This back-flow control is effected at the interrupt-level by processing initiated in any of the controllers 130, 131, ..., 132 and is passed to system interface controller 110 via the data connection interface of channel bus 111. In turn, when any program file in system interface controller 110 fills to a pre-determined level, the back-flow control is further exercised to inform signal source 150 that the particular program file can no longer accept data destined for any channel interface

controller 130, 131, ..., 132 which may have initiated back-flow control. The communication of back-flow control between system interface controller 110 and signal source 150 occurs over the data connection interface of source bus 101.

Thus to reiterate, signal processor 100, in its most fundamental implementation of inserting an advertisement into one national video feed, is arranged to receive two input signals, namely, a conventional network feed signal from the video source and a MPEG-2 digital data stream from a digital signal source, and to emit a signal composed of the network feed in one time interval and an analog version of the MPEG-2 data stream in another interval. To effect this transformation from input to output, processor 100 converts the incoming digital data stream to a video signal synchronized to the video source, controls the flow of the digital data stream between input and output, and switches from the video source to the video signal as prompted by a corresponding cue tone provided by the video source.

Details of the Signal Processing System Interface Controller

Referring now to FIG. 2, a more detailed block diagram of system interface controller 110 is shown. In one illustrative embodiment, which is the focus of the following

discussion, the SCSI 2 interface protocol implemented over source bus 101 is such that signal source 150 is the master and system interface controller 110 is the slave (or initiator and target, respectively, in SCSI 2 terminology). Thus, signal source 150 communicates with system interface controller as if processor 100 is a SCSI disk. As such, processor 100 is given an identification number (ID) as is conventional for the SCSI protocol. (In another illustrative embodiment, the roles of initiator and target are reversed; the embodiment that is deployed in any given situation depends upon the particular technical requirements of the application). The MPEG-2 compliant transport stream transmitted from signal source 150 to system interface controller 110 is processed by SCSI 2 data transport controller 205 (such as a NCR720 device supplied by SIMBIOS) which implements the system interface controller side of the SCSI protocol. The incoming transport stream is passed by data transport controller 205 to buffer memory 220 over interface bus 206; data transport controller 205 has its own DMA channel, so transport controller 205 directly moves the incoming transport stream to memory 220. Interface bus 206, in a preferred embodiment, is composed of a 32-bit data bus and a 32-bit address bus. For the case of eight channel interface controllers (130, 131, ..., 132), memory 220 is preferably 18 Mbytes of DRAM (such as a MB814260 device available from Fujitsu), with the 18 Mbytes being logically divided into nine 2-Mbyte blocks (also referred to as nine "buffers") -- a 2 Mbyte block for each channel interface

controller, and 2 Mbytes for storing processes for system processor 225 (e.g., a Motorola 68360 microprocessor). Buffer memory 220 serves as intermediate storage for channel interface controllers 130, 131, ..., 132 in that the incoming transport stream is held in 2 Mbyte queues until the data is required by the channel interface controllers 130, 131, ..., 132. Accordingly, buffer memory 220 serves to receive and divide the interleaved transport stream of incoming MPEG-2 data for delivery to the channel interface. In this capacity, system interface controller 110 functions to "de-concentrate" the incoming data stream or, from another viewpoint, controller 110 is an expander so that a plurality of channel interface controllers 130, 131, ..., 132 can be handled with only one SCSI 2 interface, thereby precluding replicated hardware as would be the case if each channel interface controller 130, 131, ..., 132 had a separate incoming data stream handled by a SCSI interface device dedicated to that separate stream.

Data stored in buffer memory 220 is retrieved under control of transfer processor 215 (e.g., a Motorola 68349 microprocessor) and passed to compressed data bus controller 210, which is illustratively a field programmable gate array (such as a XC4010 available from XILINX Inc.). Transfer processor 215 has two DMA channels which facilitate moving the data from buffer memory 220 over the 32-bit data bus of interface bus 206. Compressed data bus controller 210 places the digital data onto compressed

data bus 211, which is the logical data connection of channel bus 111 outlined in the overview discussion. Compressed data bus 211 (which will be discussed in more detail later) is composed of: an eight-bit wide data bus; an eight-bit wide select bus for selecting the channel interface controller 130, 131, ..., or 132, that is to receive the data stream emitted by the data bus; and a STATUS line. The STATUS line carries a signal which allows for the delivery of two bits of information per channel interface controller, namely, flow control and interrupt, between system interface controller 110 and channel interface controllers 130, 131, ..., 132. The status data on the STATUS line is carried by sixteen time-multiplexed slots -- two time-multiplexed slots for each channel interface controller 130, 131, ..., 132 wherein one multiplexed slot carries the flow control bit, and the other slot carries the interrupt bit. Whenever a particular channel interface controller requires data, the flow control bit is asserted to reflect the need for data which is queued in buffer memory 220 for the particular channel interface controller. Whenever a particular channel interface controller requires servicing, the interrupt bit is asserted to reflect the need for servicing.

In addition, whenever data is passed from system interface controller 110 to each channel interface controller, compressed data bus controller 210 converts each 32-bit data into four 8-bit data words for byte-wide serial

transmission over compressed data bus 211. The particular channel interface controller that is to receive the serial data is determined by the location of the serial data in memory 220, that is, in which one of the eight 2-Mbyte blocks the data is stored.

The data and address buses comprising bus 206 are subject to being mastered by three different devices, namely, data transport controller 205 and system processor 225 as well as transfer processor 215. Arbitration logic 226 (e.g., a field programmable gate array such as a Lattice 3256 ispLSL) couples data transport controller 205, transfer processor 215, and system processor 225 to effect arbitration among the potential master devices. Arbitration logic 226 prevents one master from dominating the other possible masters. For instance, system processor 225 can only be master for a pre-determined number of clock cycles (e.g., 16), and then the other possible masters may contend for interface bus 206.

With respect to the control connection function of source bus 101, the incoming Ethernet link terminates in system processor 225. This link, for instance, is used to transfer cue tone information to signal source 150 so source 150 can select and schedule the advertisement for insertion. The control connection on the channel interface controller side of system interface controller 110 is provided by control bus controller 230, which is

illustratively a field programmable gate array (e.g., a Lattice 1048c device); bus controller 230 is coupled to channel bus 111 via control bus 212, which supports the logical control connection of channel bus 111. Control bus 212 (which will be discussed in more detail later) is composed of: an 8-bit wide control data bus; a 10-bit wide control address bus; a 3-bit wide select bus; and a read/write (R/W) lead. The 3-bit select bus allows for the accessing of the eight channel interface controllers, typically on a polling basis or in response to an interrupt request. The R/W lead allows for writing data to each channel interface controller 130, 131, ..., 132 (e.g. via channel processor 265 of channel interface controller 130); in addition, channel interface controller 130 can pass information back to bus controller 230 as directed by the R/W lead. Bus controller 230 accomplishes the function of translating 32-bit data to 8-bit data required of channel interface controllers 130, 131, ..., 132, and vice versa.

In addition, system processor 225 can arbitrate, via arbitration logic 226, into the address space of data transport controller 205 thereby leaving messages/data in memory 220 for data transport controller 205 or by retrieving messages/data from data transport controller 205 (via the 2 Mbyte block reserved for processes of system processor 225). Thus, system processor 225 has indirect access to each device which data transport controller 205 may access.

Moreover, system processor 225 also controls modulator bus 108, and each individual carrier frequency for the RF modulation of the output signal produced by each channel interface controller 130, 131, ..., or 132 is set by system processor 225.

Thus to reiterate, system interface controller 110 is implemented as an inter-dependent, two-processor arrangement (namely, transfer processor 215 and system processor 225) wherein the resources of system processor 225 primarily perform the managing and scheduling functions for delivery of the incoming interleaved MPEG-2 data stream to the desired ones of the channel interfaces controllers 130, 131, ..., 132, and wherein the resources of transfer processor 215, in conjunction with data transport controller 205, are dedicated to handling the incoming data transfers because of the high throughput rate required. This two-processor architecture allows for the delivery of the appropriate data streams to a plurality of channel interface controllers 130, 131, ..., 132, thereby effectively spreading the cost of one SCSI drive over a plurality of channel interface controllers. (This is in contrast to conventional arrangements wherein there is a one-to-one correspondence, rather than a one-to-many correspondence, between the intelligence and the decoding functions, that is, normally a single processor is dedicated to each channel.)

Channel Interface Controller

Referring again to FIG. 2, a more detailed block diagram of one channel interface controller (say controller 130) is shown. The block diagram of controller 130 focuses on data flow and signal flow which are essential to generating audio and video analog signals from digital input data. During transmission of the programming from video source 160 via input channel 102 to channel interface controller 130, break periods designated for commercial advertisements are denoted by cue tones which arrive over a separate path (not shown) in channel 102. The cue tones indicate that insertion of a commercial advertisement by the local programmer is called for at a specific time; typically, cue tones are in DTMF format. (In the discussion that follows, in order to exemplify with specificity the processing engendered by the arrival of cue tones, the following case is considered. It is supposed that only the "pre-roll" cue tone is required, and ad-insertion switches (transfer-to-ad and return-from-ad) may be keyed off the pre-roll cue tone. Such would be the case if a given national feed operator fixes, at pre-set values, the pre-roll interval and the duration of each break. Cases wherein the other cue tones may be utilized will be readily understood by those with ordinary skill in the art.)

Cue tone controller 280 receives its input from channel input 102 and detects the presence of a pre-roll cue tone in the incoming signal provided by video source 160. The detection of the pre-roll cue tone is reported to channel processor 265 (e.g., a Motorola 68306 microprocessor) via lead 281. Once a pre-roll cue tone is detected, cue tone information representative of the pre-roll cue tone and channel sequence is passed from channel processor 265 to system interface controller 110 via the control bus portion (i.e., bus 212) of interface bus 111 and, in turn, to source 150 via the Ethernet portion of source bus 101. Source 150 is able to identify the particular national channel being serviced by channel interface controller 130 from the cue tone and channel information. Moreover, based on the time-of-day (i.e., a real-time clock), source 150 is further able to identify the commercials to be inserted in the particular break interval. Such commercial information has been pre-loaded via an off-line, pre-processing step which loads source 150 with the digital data representative of the advertisement inserts needed by all channel interface controllers over a pre-determined time interval (e.g., a 24 hour period). The advertisement to be inserted is retrieved as a MPEG-2 transport stream from the storage device component of signal source 150. The retrieved advertisement is provided to system interface controller 110 via source bus 101 and, in turn, after storage and processing by system interface controller 110 as presented in the foregoing section, to

transport DEMUX 235 (e.g., a CL9110 device manufactured by C-Cube Microsystems) via the compressed data bus portion (i.e., bus 211) of interface bus 111.

The MPEG-2 transport stream representative of the retrieved advertisement is prepared as a MPEG-2 transport stream composed of MPEG-1 or MPEG-2 compliant elementary data streams. This transport stream is the interleaved digital data stream emitted by source 150 to system interface controller 101 destined for all channel interface controllers 130, 131, ..., 132, and portions of this interleaved digital data stream is the stream ultimately received by DEMUX 235 for controller 130, which then separates the transport stream into MPEG elementary data streams representative of, for example, audio information and video information. The separated data streams are temporarily stored in the memory portion of and controlled by DEMUX 235. More specifically, the MPEG-2 transport stream is characterized by a MPEG packet having a transport "header" and a payload portion, that is, an elementary data stream. DEMUX 235 first synchronizes to conventional MPEG packet boundaries and, once synchronized, then parses the packet to obtain header information and routes the payload to its storage. The transport header indicates what type of information is contained in the packet, such as audio, video, secondary audio programming (SAP, to be discussed later), and private data. The payload is stored in different areas of DEMUX's 235 memory based on the type of

information in the payload; e.g., the video is stored in an queue which is proportionately larger than the memory allocated to audio and SAP due to the large number of bits required to generate the video component of the overall output signal compared to the audio component.

1. Video Processing

Now, with respect to the video processing portion of channel interface controller 130, the video data stored in the video queue of DEMUX 235 is available to MPEG video decoder 250 via path 236. Decoder 250 (e.g. a STi3500A MPEG Video Decoder manufactured by SGS-Thomson Microelectronics) also is composed and controls its own memory, and if its memory is not full so it can accept video data (known to DEMUX 235 via a hardware-type "handshake" over path 236), then DEMUX 235 downloads video data to video decoder 250 for storage in its memory. Thus, from the description to this point, it is clear that the video data, besides being initially stored in digital source 150, is also stored in three intermediate memories, namely, buffer memory 220 of system interface controller 110, the video storage of DEMUX 235, and the video storage of video decoder 250. The storage algorithm is such that the receipt of the pre-roll cue tone causes: (1) the memory of video decoder 250 to be fully loaded first; (2) next, the memory of DEMUX 235 is fully loaded, but only after the memory of video decoder 250 is fully loaded; and (3) buffer memory 220 is fully loaded,

but only after the memory of DEMUX 235 is fully loaded. With this algorithm, the data needed to generate the analog version of the commercial advertisement is distributed within the overall system 100 to optimize local analog video generation in a timely manner for immediate substitution of the local advertisement in the national video signal during the scheduled break interval.

As outlined earlier, a normal MPEG-2 transport stream is emitted with the presumption that downstream circuitry is arranged to handle the transport stream without loss of incoming data bits. As just pointed out in the discussion of the cascade of three intermediate memories, it is possible during the pre-roll interval to fill all intermediate memories before any of the data is required to generate the ad-insertion analog signal. Thus, a back-flow control mechanism to control the MPEG-2 transport stream is necessary to ensure no data bits from the transport stream are lost. One embodiment of the back-flow algorithm may be characterized as follows. DEMUX 235 and video decoder 250 use a hardware handshake to determine when the memory of decoder 250 is full. Channel processor 265 monitors the storage of DEMUX 235 to determine when its storage is full, which impliedly means that the storage of video decoder 250 is also full. When DEMUX 235 can no longer accept data for storage, channel processor 265 conveys this information to transfer processor 215 of system interface controller 110 via the compressed data bus portion (i.e., bus 211) of

interface bus 111 (in particular, the STATUS line). In turn, transfer processor 215 inhibits transfer of data to DEMUX 235 via compressed data bus controller 210. Buffer memory 220 begins to fill, and once full to a pre-determined level, data transport controller 205 informs source 150, using the SCSI-2 protocol, that transport controller 205 cannot accept another MPEG-2 transport stream over source bus 101 bound for controller 130. Source 150 truncates the transmission of transport streams to system interface controller 110 for the given channel interface controller (here controller 130). Then source 150, for example, performs "round-robin" polling of other channel interface controllers for servicing. Upon returning to controller 130 (which previously blocked a transport stream in this example), source 150 will again attempt to transmit the same transport stream that was rejected earlier. This stream may be accepted if the intermediate buffers have emptied, or the stream may again be rejected. Source 150 continues its "round-robin" processing.

As mentioned, the particular lead from compressed data bus 211 that is used to carry back-flow information from channel interface controller 130 to system interface controller 110 is the STATUS lead. In one embodiment, the STATUS lead is divided into 16 time-multiplexed slots -- 2 for each of eight channel interface controllers. One of the two slots is used for the back-flow control; for instance, a "0" bit would indicate that DEMUX 235 can accept a transport

data stream, whereas a "1" bit would indicate that the storage of DEMUX 235 is full. The other one of the two slots, in one embodiment, is used to signal system processor 225 of system interface controller 110 that channel processor 265 needs servicing, that is, this other slot carries an interrupt request. The communication which occurs over the STATUS lead is asynchronous with respect to any data being transmitted over the data leads of compressed data bus 211, that is, either or both the flow control and interrupt request can occur independently in time relative to the transmitted data.

Continuing with the video processing portion of FIG. 2 for the selected advertisement now assuming that an analog signal is to be immediately constructed from the incoming digital data stream, it is presumed that the compressed digital data stream has been delivered from DEMUX 255 to MPEG video decoder 250 as elementary video streams. Video decoder 250 decompresses the video signal in MPEG format to a decompressed digital video signal appearing on path 251, which serves as one input to video encoder 255 (e.g., a SAA7185A Video Encoder manufactured by Phillips Semiconductors). A second input to video encoder 255 is illustratively a 27 MHz clock signal from Genlock controller 270; the origin of the 27 MHz clock is discussed in more detail shortly. With this clock signal, video encoder 255 encodes the incoming digital video signal on path 251 in a transmission format such as a NTSC composite

video signal, and thus converts the digital signal to an analog video signal appearing on path 256. The analog video signal on path 256 serves as one input to video switch 260.

For the illustrative embodiment depicted in FIG. 2, the cascade arrangement of MPEG video decoder 250 followed by video encoder 255 is required so as to convert from one standard (MPEG) to another standard (NTSC composite). This conversion can be understood from a consideration of what information is provided by each MPEG elementary stream and what format is necessary for transmission of the advertisement to the television receiver of the local viewer. The NTSC composite signal is composed of a video signal having, for example, the R, G, B color component information placed appropriately onto a single lead in path 256. Broadly, the NTSC encoding process is defined as the process of converting the R, G, B color components (or the Y, U, V equivalents) available individually into a composite video signal for transmission over a single wire. The MPEG video encoder 250, on the other hand, delivers the equivalent of the R, G, B components as three individual components Y, U, V as time-multiplexed signals appearing serially onto a single byte-wide bus (path 251 of FIG. 2). Thus, MPEG video decoder 250 and NTSC video encoder 255 complement each other to effect the necessary conversion from the MPEG standard to the NTSC composite signal standard.

The analog video signal from video source 160 appearing on input channel 102 is supplied to level adjust circuit 275, which accomplishes two functions, namely: (1) provides automatic gain control to restore the signal strength of the incoming network feed signal to a pre-determined value if the incoming signal is attenuated; and (2) shifts the level of the gain-controlled network video signal as needed to ensure that the "back porch" of the video signal is properly set at zero volts. As is well-known in the art, the "back porch" of a video signal is the interval of a video waveform between the end of the horizontal synch pulse and the beginning of the active video information. The clamped video signal, appearing on path 276, is a second input to video switch 260. Genlock controller 270 recovers the original timing control signals (such as horizontal synch, vertical synch, and color subcarrier) from the gain-controlled network television signal appearing on path 276. The output of Genlock controller 270 is illustratively a 27 MHz clock and vertical and horizontal timing signals in horizontal and vertical synchronization and in-phase with the network feed signal on channel 102. Genlock controller 270 supplies these timing and synchronization signals to audio encoder 240 and video encoder 255 via path 271. Thus, the MPEG decoding operations performed by audio encoder 240 and the combined decoding/encoding operations performed by the cascade of decoder 250 and encoder 255 are performed according to the clock generated by Genlock controller 270 rather than a

clock which is embedded in the MPEG-2 data stream. By using the clock recovered from the network television signal to perform MPEG decoding/encoding, synchronization between the national video source and the reconstructed video signal from the MPEG-2 data stream may be achieved, thereby precluding vertical roll and other problems which might otherwise occur as a result of switching between the national feed and the converted MPEG-2 data stream.

Now with reference to FIG. 3, a more detailed block diagram of the forward digital data and signal flow for the video processing portion of channel interface controller 130 is shown. The video portion of the national video signal appearing on channel 102 serves as the input to automatic gain control (AGC) circuit 320 so as to compensate, if necessary, for any signal loss during transmission over channel 102. The gain-controlled video signal produced by AGC 320 is supplied to "black level" clamp circuit 322 to fix the black level of the national video signal at the reference level of zero volts. The clamped output of clamp circuit 322 is provided as one input to video switch 260 on path 276-1, that is, on one of the sub-paths comprising path 276. The gain controlled video signal from AGC 320 is also provided as an input to synch strip circuit 324, which generates synchronization information, including horizontal synchronization appearing on path 276-2 and vertical synchronization information appearing on path 276-3. Synch strip circuit 324 also

develops a control voltage proportional to the amplitude of the output of AGC circuit 320 which is fed back, as a negative feedback signal, to AGC circuit 320 so as to increase or decrease the gain as needed to restore the network video signal to a given amplitude at the input to a conventional receiver. Synch strip circuit 324 also supplies a "back porch" timing signal to "black level" clamp circuit 322, that is, the "back porch" timing signal indicates when the "back porch" of the national video signal occurs so the black level may be set.

The horizontal synch signal appearing on path 276-2 serves as an input to Genlock controller 270; components comprising one illustrative embodiment of Genlock controller 270 are also depicted in FIG. 3. In particular, the horizontal synch signal on path 276-2 is supplied to phase detector 330 which feeds low-pass filter 334. The output of filter 334 serves as the input to voltage controlled crystal oscillator (VCXO) 336 which is set to run, in the preferred embodiment, at 27 MHz ± 25 ppm. The output of VCXO 336 is supplied to 54 MHz phase-locked loop (PLL) circuit 340, and the output of PLL 340 is then divided in half by division circuit 344 to produce an output signal of 27 MHz having a 50% duty cycle. As is standard in the art, a 50% duty cycle is required by certain integrated circuits for proper signal processing. PLL 340 and division circuit 344 may be realized, illustratively, by a MC88915 device manufactured by Motorola.

Phase detector 330 compares the frequency and phase of the horizontal synchronization information appearing on path 276-2 with the frequency and phase of a regenerated horizontal synchronization signal appearing on lead 271-1 produced by video encoder 255 (as described in more detail shortly), and generates an output control voltage based on the comparison. This control voltage is filtered by low-pass filter 334, and then the output of filter 334 is used to adjust the phase and frequency of VCXO 336 so the regenerated timing signal appearing on path 271-1 at the input to phase detector 330 has the same phase and frequency as the national video feed signal; the signal on path 271-1 is used by logic 306 to encode the decompressed digital video information into, for example, the NTSC composite signal format. Phase detector 330 also generates a "lock-detect" signal 271-3 whenever the compared phases are substantially identical, and supplies this "lock-detect" signal to channel processor 265 over bus 111 to control signal processing by channel processor 265.

The 27 MHz signal from Genlock controller 270 is supplied as a clock signal to horizontal counter (Hcntr) circuit 304 of video encoder 255 via path 271-2; in addition, the vertical synchronization information from synch strip circuit 324 is supplied to vertical counter (Vcntr) circuit 302 via path 276-3. Finally, the decompressed digital video information from MPEG video decoder 250 is supplied to video encoder 255 via path 251.

In particular, the compressed data formats arriving at DEMUX 235 over channel bus 111 are MPEG-1 and MPEG-2 elementary streams which are packetized and layered in an MPEG-2 transport stream. Video decoder 250 decodes Main Level/Mail Profile streams at up to 15 Mbps for each channel 130, 131, ..., 132. Horizontal resolutions include up to 720 pixels per line and are sample-rate converted to CCIR601 resolution for presentation, via input path 251, to video encoder 255 so as to generate, for example, composite analog NTSC signal appearing on lead 256-1 (a sub-path of path 256).

The vertical synchronization information provided to vertical counter 302 is used to reset vertical counter 302 once per field (or once per frame, depending upon the desired format). The 27 MHz information supplied to horizontal counter 304 increments horizontal counter 304 each clock cycle until the counter reaches a value, for the NTSC format, of 1715 (that is, 1716 counts -- this value may be modified as necessary for other formats such as PAL), whereupon counter 304 is reset to zero. Each time horizontal counter 304 is reset, vertical counter 302 is simultaneously incremented by one to start a new video display line; vertical counter 302 is reset after one full frame of 525 lines (that is, counter 302 counts from 0 to 524). The outputs of counters 302 and 304 are supplied to logic circuit 306, which also generates the conventional composite synchronization and the color subcarrier signals;

in turn, the composite synchronization and color subcarrier signals are supplied, along with the decompressed digital video information from MPEG video decoder 250, to digital video encoder circuit 308, which is the element of video encoder 255 to actually effect the conventional digital encoding for NTSC transmission. The NTSC-encoded digital information is then converted to analog information via digital-to-analog (D/A) converter 310, which generates an analog video signal representative of the incoming MPEG-2 data stream having substantially the same vertical synch as the network video feed signal. Filter 312 is a low-pass analog filter which smoothes the staircase characteristic of the signal from D/A converter 310. The filtered analog video signal is then applied to DC restore circuit 314 to clamp the black-level to zero volts. The clamped analog signal is then applied to gain circuit 316 which is adjusted to zero out amplitude and offset errors caused by variations in nominal characteristics of video encoder 255. The output of gain circuit 316, which appears on lead 256-1, is the second video input to video switch 260. It is also noted, as alluded to above, that logic circuit 306 is that part of video encoder 255 which provides re-generated horizontal synchronization information, via path 271-1, to phase detector 330 for comparison to the horizontal information produced by synch strip circuit 324.

Video switch 260 receives a control signal from channel processor 265 via bus 268, in response to a given

cue tone, so that the output from switch 260 is either the clamped, gain-controlled national analog video feed or the decompressed and converted video signal supplied by the signal source 150 -- both the video feed and video signal have the same phase and vertical and horizontal synchronization signals by virtue of the overall processing effected by channel interface processor 130. Preferably, the switch between the national video feed (path 276-1) and the video signal on lead 256-1 generated from signal source 150 occurs during the vertical blanking interval (VBI) of the national video feed. The VBI is a time period during which the television picture scanning beam is "blanked" so that it may be returned from the bottom of the television screen to the top of the screen without being visible to the viewer. To ensure that the switching operation occurs during the VBI for both switching from and back to the national video feed, the national video feed is monitored at all times by Genlock controller 270, including during transmission of the MPEG-derived signal. Preferably, logic circuit 306 generates and provides such vertical timing information to video switch 260 via lead 256-2 of path 256.

2. Audio Processing

Now with respect to audio processing, reference is again made to FIG. 2. Audio encoder 240 receives the audio information, decompresses and converts the audio information

to a digitized audio signal and, in turn, converts the digitized audio signal to a reproduced audio signal via standard digital-to-analog conversion. The reproduced audio signal appears on path 241, and serves as one input to audio switch 245; a second input to audio switch 245 is provided by video source 160 via incoming channel 102. The decompression and conversion of the digital audio information are performed under control of Genlock controller 270, which effects a stable clock signal (e.g., 27 MHz) on path 271, as based on the timing information provided by video source 160. The 27 MHz clock controls the rate at which the decompressed incoming digital audio signal is decompressed, and controls the rate at which the decompressed digital information is converted to analog audio information.

Reference is now made to FIG. 4 for a discussion of sub-components of audio processing circuitry 240, including sub-circuits 2410 and 2411, for an illustrative embodiment of the present invention. In particular, path 237 coupled to DEMUX 235 delivers compressed data signals Lc and Rc which are representative of the left channel and right channel audio signals, respectively, of the advertisement to be inserted into the national network feed supplied by incoming national feed channel 102. The compressed data signals on path 237 serve as inputs to audio decompressor 2401, which includes internal counter 2403. The re-generated 27 MHz clock signal appearing on lead 271

serves as another input to audio decompressor 2401 and, in particular, is used to control the incrementing of counter 2403. Counter 2403 may be loaded with an initial value via path 238, as described in more detail shortly.

The outputs of audio decompressor 2401, designated Ld and Rd for left and right digital signals, respectively, are the decompressed counterparts of Lc and Rc; Ld and Rd serve as inputs to dual-channel D/A converter 2402. The outputs of converter 2402 are the left and right analog signals La and Ra appearing on leads 241-1 and 241-2, respectively. La and Ra are the reconstructed analog audio signals corresponding to the compressed digital data signals Lc and Rc, respectively; La and Ra serve as inputs to audio switch 245. Two other inputs to audio switch 245, appearing on channel 102, are the left and right (L and R) audio signals provided by the national network feed signal. Analogous to the video processing described above, audio switch 245 is switched, under control of channel processor 265 via bus 268, from the national network feed to the ad insertion path and vice versa based upon the detection of the pre-roll cue tone signal, wherein such switching occurs at such instants to avoid video roll in downstream or customer TVs tuned to the TV channel under consideration.

Circuitry 2410 is, illustratively, device CS4920A supplied by the Crystal Corporation; this device is an

off-the-shelf device that includes the circuitry necessary to properly decompress audio digital data, synchronize the audio to the video (called AV synch), and effect digital-to-analog conversion. Circuitry 2411 of FIG. 4 is also device CS4920A, and its purpose and function will be discussed shortly.

In order to synchronize the audio portion and the video portion (AV synch) of an inserted advertisement, the video and audio processing paths are coupled in the following manner. With reference to FIG. 2, it is recalled that the video portion of the ad insertion is provided over path 236 to video decoder 250, and the audio portion of the ad insertion is provided over path 237 to audio encoder 240; the video and audio portions arrive via an MPEG-2 transport stream which has interleaved video and audio packetized elementary data streams that are stored in separate areas in memory of DEMUX 235.

In normal MPEG-2 operation, the headers of the packetized data streams have embedded timing information -- called presentation time stamps (PTSs) which are placed periodically into the video and audio streams by the encoding operation using an encoder clock which drives the encoding processing. Moreover, in MPEG-2 operation, the transport headers have overall timing information -- called program clock regenerators (PCRs) which are placed periodically into the transport stream so as to enable the

regeneration of a clock signal at a decoder which can be used to drive the decoding process. Accordingly, by comparing the PTS from a video or audio stream with the clock derived from the PCRs, it is possible to emit a reconstructed video frame and corresponding audio signal, in synchronism, from the decoder.

As elaborated on in the foregoing material for the present invention, the 27 MHz decoding clock for video and audio processing is derived from the incoming national feed signal. Moreover, the instant in time at which ad insertion is to occur is controlled, not by the PCRs of the MPEG-2 stream in conjunction with the PTS of the packetized elementary streams, but by count-downing from the cue tone based upon the given pre-roll time. Since the first video frame is, by the storage algorithm presented above, already stored in video decoder 250, the PTS of the first video frame is known. According to the operation of the present invention, at the instant that the first video frame is switched through encoder 255 to switch 260 for ad insertion, the PTS of the first video frame is loaded into counter 2403 of audio encoder 240 (see FIG. 4), and counter 2403 increments under control of the 27 MHz clock on lead 271. The PTS's of the incoming audio elementary stream are then compared to the contents of counter 2403, and when any PTS is equal to the counter's contents, the audio compressor activates to convert Lc and Rc to La and Ra, respectively, to achieve AV synch.

To complete the description of FIG. 4, reference is made to circuitry 2411 in the lower portion of FIG. 4. The operation of circuitry 2411 is substantially the same as circuitry 2410, except now there is only one input to audio decompressor 2405, namely, SAPc (which is shorthand for compressed Secondary Audio Programming, such as compressed audio in Spanish) from bus 268. The SAPc signal is also delivered as a packetized elementary stream, but in contrast to the video and audio compressed data appearing on leads 236 and 237, respectively (see FIG. 2), SAPc is provided via an indirect path which includes: storage initially in memory of DEMUX 235; retrieval of the compressed data from the storage of DEMUX 235 under control of channel processor 265 via bus 266; and delivery of the compressed data as the SAPc signal to audio decompressor via bus 268. In the same manner as described above, the PTS's on the incoming SAPc signals are used to enable AV synch for the SAP path, that is, the PTS's are used to convert SAPc to SAPd (decompressed SAP digital data) and, in turn, to convert SAPd to SAPa (analog SAP) at the input to switch 245 on lead 241-3. Thus, switch 245 delivers, in parallel on path 246, either the national feed signals L-R-SAP or the signals La-Ra-SAPa derived from signal source 150.

3. Interconnection Between System Interface Controller and Channel Interface Controller

The circuit diagrams of FIGS. 5 and 6 show the pertinent leads composing compressed data bus 211 and control bus 212 for a system with eight channel interface controllers. Compressed data bus 211 includes: (a) eight data leads forming byte-wide bus 505; (b) a plurality of select leads forming select bus 510, wherein the number of select leads equals the number of channel interface controllers 130, 131, ..., 132; and (c) STATUS lead 515 which, as set forth above, provides control information from the plurality of channel interface controllers 130, 131, ..., 132 to system interface controller 110 over a plurality of time-multiplexed intervals. In particular, for a system with eight channel interface controllers 130, 131, ..., 132, there are eight time-multiplexed intervals, with each interval being subdivided into two slots for each controller (for a total of sixteen slots), with the first slot of each interval carrying the interrupt request from the given controller, whereas the second slot carries the flow control information for the given controller.

Similarly, control bus 212 is composed of: (a) eight data leads forming byte-wide bus 650 and a corresponding data strobe lead 651; (b) a plurality of address leads forming bus 665 in correspondence to the size of memory of a dual-port RAM (shown in FIG. 9 as

element 267) comprising channel processor 265 in each channel interface controller 130, 131, ..., 132; (c) a plurality of select leads forming bus 660 in correspondence to the number of channel interface controllers 130, 131, ..., 132; and (d) read/write (R/W) lead 665 alluded to above for communicating between each channel interface controller 130, 131, ..., 132 and system interface controller 110. In particular, for eight channel interface controllers 130, 131, ..., 132, there are three select leads forming bus 660 to thereby uniquely select any one of the eight channel interface controllers during a given processing cycle. Also, if the dual-port RAM has 1024 memory locations, then the number of address leads in bus 665 is ten to thereby uniquely access any desired location in the dual-port RAM.

To further elucidate the back-flow control method in accordance with the present invention, reference is made to FIG. 7, which shows the relevant circuitry for communicating back-flow control information from channel interface controller 130 to system interface controller 110. It is supposed that the memories of MPEG decoder 250 and transport DEMUX 235 used to store video information are full (e.g., in preparation for inserting an advertisement in the network feed in response to a cue tone), and that it is necessary to inform system interface controller 110 of the status of the memories. Channel processor 265, which monitors the memory of DEMUX 235 to determine the remaining

storage capacity of its video, audio, SAP, and private data areas, has determined that DEMUX 235 cannot accept any incoming video data over data bus 505 of compressed data bus 211. Channel processor 265 inserts a "1" bit into its allocated slot on STATUS lead 515, that is, into the second of sixteen slots carried by STATUS 515 for a system of having eight channel interface controllers and wherein channel interface controller 130 is designated as the first controller in the grouping (indicated by #1 in FIG. 7). Lead 515 of compressed data bus 211 delivers the asserted bit to compressed data bus controller 210 in system interface controller 110. In turn, controller 210, using interface bus 206, relays this flow control information and the particular channel interface controller transmitting the flow control bit (known by its location in the time-multiplexed stream on STATUS lead 515) to transfer processor 215 so as to turn-off its transmission of data from memory 220 over interface bus 206 to compressed data bus controller 210 (via processor 215's DMA capability).

It is further supposed, as portrayed in FIG. 8, that eventually the memory area allocated to controller 130 in memory 220 becomes filled to, at least, a pre-determined level (say one-half full) since controller 130 can no longer store data originating from memory 220. Transfer processor 215 receives an indication over interface bus 206 that memory 220 also can no longer accept data destined for channel interface controller 130, and relays this indication

to data transport controller 205 via bus 206. Signal source 150 is arranged to handle each of the buffers in memory 220 corresponding to each channel interface controller 130, 131, ..., 132 as a logical disk so that standard SCSI-2 commands can be used to write each separate buffer in memory 220. The SCSI-2 driver software is executed by transfer processor 215 and controls data transport controller 205; this driver is arranged to manage a "write" from signal source 150 in the following manner. On every write from signal source 150, this driver returns a "status" signal indicating the "fill level" for the current buffer in memory 220 that is being written to by signal source 150. The driver inhibits a write to a buffer that is full to a pre-determined level. With this status indication, signal source 150 can adjust the rate of data transfer to the given buffer. Whenever the buffer is free to again be re-written, a status signal informs signal source 150 of this condition, so a re-send of the previously denied data block may be re-transmitted. As outlined earlier, source 150 then "round robins" to determine which remaining channel interface controllers may accept MPEG-2 transport streams, that is, those channel interface controllers which have not asserted back-flow control.

Now, to further elucidate the processing of an exemplary interrupt request by a channel interface controller over STATUS lead 515, reference is made to FIG. 9, which depicts the relevant circuitry for

communicating the interrupt request from channel interface controller 130 to system interface controller 110. It is supposed that cue tone controller 280 has detected the presence of a pre-roll cue tone in incoming path 102 from the national video feed. Controller 280, typically via an interrupt request over lead 281, passes the indication of such a cue tone (C) plus information about the tone, that is, its representation in DTMF format, to channel processor 265. For the sake of specificity, presume that the detected tone is indicative of the letter "N" (for, say, NBC). Channel processor 265 starts a count-down clock that will initiate the timing of the ad insertion, places both the indication and information in an agreed-upon, predetermined location (e.g., the C"N" information location 100 as shown in FIG. 9) in dual-port RAM 267, and then changes the interrupt bit from a "0" to a "1" in the first of the sixteen slots (the one assigned to the interrupt request for channel interface controller 130) on STATUS lead 515. The interrupt request in passed to compressed data bus controller 210 in system interface controller 110 which, in turn, passes the interrupt request to system processor 225 over interface bus 206. Interface processor 225 provides control bus controller 230 with information which allows controller 230 to access the data stored in location 100 of dual-port RAM 267. Accordingly, control bus controller 230 operates to select channel interface controller 130 via select bus 660, to access location 100 in RAM 267 via address bus 655, and to read the

data from location 100 via data bus 650 upon assertion of R/W bus 665 and as signaled by strobe lead 651. The information arriving over control bus 212 is passed to system processor 225 via bus controller 230.

System processor now passes the information to signal source 150 using any standard protocol (e.g., TCP/IP) over Ethernet link 101-2. Signal source 150 uses this information to identify and select the advertising information that is to be downloaded to channel interface controller 130 for ad insertion.

Overview of Signal Processing

As set forth in the foregoing description of signal processor 100 in accordance with the present invention, there are typically a plurality of autonomous, distributed processors executing simultaneously, but wherein the execution of each of the processors may depend upon control signals originating in one or more of the other processors. In particular, there are illustratively ten processors in signal processor 100 of FIG. 1 for a system having eight channel interface controllers, namely: transfer processor 215 and system processor 225 in system interface controller 110; and one channel processor 265 in each of eight channel interface controllers 130, 131, ..., 132. Moreover, there is generically one processor (not shown) in signal source 150. The presentation below provides a

description of the operation of each of these processors and its interaction with the other processors using both a state-diagram approach as well as a flow chart approach to completely elucidate the interaction among processors.

Interaction of Signal Processing

The state-diagram of FIG. 10 shows a high-level state diagram for the interaction of tasks (shown in circles) to effect the transfer of data from signal source 150 upon the arrival of cue tone information. The tasks are shown as executing in the two processors of system interface controller 110 and one channel interface controller 130 comprising signal processor 100, as well the tasks of signal source 150. In particular, an ad insertion process is initiated whenever an appropriate pre-roll cue tone arrives on lead 102 (FIG. 1) and is passed to cue tone task 1005 of channel processor 265 via an interrupt on lead 281. Cue tone task 1005 determines the validity of the pre-roll cue tone and, if valid, cue tone task 1005 sends the cue tone information to control data bus task 1010. Control bus task 1010 stores cue tone information in dual-port RAM 267 (FIG. 9) and passes an interrupt message over STATUS lead 515 (FIG. 5) to compressed data bus task 1050 upon storage of the complete cue tone information. In turn, compressed data bus task 1020 of system processor 225 handles the interrupt service request generated by compressed data bus task 1050, and determines

the information needed to access the proper channel interface controller from information transmitted over STATUS lead 515. System processor 225 access the cue tone information from dual-port RAM 267 via control bus task 1015. Control bus task 1015 passes the cue tone information to Ethernet task 1025 of system processor 225 and, in turn, to Ethernet task 1030 of signal source 150. The processing by signal source 150 generates an MPEG-2 transport stream for propagation over SCSI bus 101-1 (FIG. 8) via SCSI task 1035 invoked by signal source 150 and associated SCSI task 1040 operational in transfer processor 215. SCSI task 1040 passes the MPEG-2 transport stream to controller 130 (FIG. 1) via compressed data bus task 1045 in transfer processor 215 and the companion compressed data bus task 1050 in channel processor 265. In turn, the transport stream is passed to transport task 1055 which is a high-level task controlling the operation of the cascade of DEMUX-decoder-encoder for both audio and video as described with reference to FIGS. 1-9. Transport task 1055, when invoked, supplies the back-flow control signal to compressed data bus task 1050 whenever DEMUX 235 (FIG. 3) can no longer accept the MPEG-2 transport stream over compressed data bus 211 (FIG. 5). This back-flow control signal is transmitted, a seriatim, to compressed data bus task 1050 and compressed data bus task 1045. Whenever memory 220 of system interface controller 110 (FIG. 1) can no longer accept the MPEG-2 transport stream destined for channel interface controller 130, SCSI task 1040 is invoked

to inform SCSI task 1035 to stop the flow of the MPEG-2 transport stream for channel interface controller 130. SCSI tasks 1035 and 1040 coordinate to re-initiate the transmission of the MPEG-2 transport stream wherever memory 220 empties sufficiently to store data delivered by the MPEG-2 transport stream data.

The flow diagrams of FIGS. 11-13 are the counterpart of the task processing described with reference to FIG. 10. In particular, referring now to flow diagram 1100 of FIG. 11, after initialization block 1105 is executed, processing by decision block 1110 is initiated to await the detection of an incoming pre-roll cue tone. An incoming pre-roll cue tone invokes interrupt block 1115 to pass an interrupt to channel processor 265 to signal the arrival of a cue tone. Decision block 1120 is invoked to determine when all incoming cue tone information has been received from cue tone controller 280. Once the cue tone information has been correctly received, processing block 1125 is invoked to load the cue tone information in dual-port RAM 267. Then, an interrupt signal is transmitted over STATUS lead 515, as depicted by processing block 1130. Next, system processor 225, in response to the interrupt signal, reads the information from dual-port RAM 267 under control of processing block 1135. In turn, as evidence by processing block 1140, system processor 225 communicates with signal source 150 via Ethernet link 101-2 to pass along the cue tone information. Server 150, via processing

block 1150, parses the cue tone information to identify the locations in the database of signal source 150 which store the appropriate MPEG-2 data for delivery to the corresponding channel interface controller (in this example, controller 130) that initiated the request.

Continuing now with flow diagram 1200 of FIG. 12 (continued block 1155 couples to continuation block 1205), processing block 1210 is invoked to retrieve that identified MPEG-2 data and, in turn, processing block 1215 transmits the retrieved data as part of the MPEG-2 transport stream carried by SCSI-bus 101-1. Next, processing block 1220 is invoked to store the retrieved data in the buffer of memory 220 assigned to channel interface controller 130; processing block 1230 indicates that the buffer for channel interface controller 130 is extracted and then transmitted over compressed data bus controller 210 via direct memory access executed by transfer processor 215. During the storage, retrieval, and transmission of data in memory 220, decision block 1225 is executing to monitor for the assertion of the back-flow control over STATUS lead 515 to inhibit the flow of data from memory 220 to channel interface controllers 130, 131, ..., 132. As depicted by processing block 1235, the incoming MPEG-2 data stream to channel interface controller 130 is parsed into elementary streams and the parsed data is stored in DEMUX 235 into, for example, separate video, audio, SAP, and private data storage areas.

Continuing with flow diagram 1300 of FIG. 13, which depicts the processing for the video portion of the ad insertion signal (video block 1240 of FIG. 12 couples to video block 1305 of Fig. 13), decision block 1310 detects if the hardware handshake between DEMUX 235 and MPEG video decoder 250 indicates that video decoder 250 can no longer accept data. Whenever MPEG video decoder 250 can accept data, processing by block 1315 is initiated to load the memory of decoder 250 with data from the video storage in DEMUX 235. Next, decision block 1320 is entered to determine the instant at which a switch-to-ad signal is to be effected. As evidenced by processing block 1325, upon a switch-to-ad indication, MPEG decoder 250 transmits the digital data stream representative of contiguous frames of the inserted advertisement to video encoder 255 for processing. In turn, processing block 1330 is invoked so that video encoder 255 converts the incoming time-multiplexed digital data stream to a composite video signal (such as NTSC). The synchronized video frames produced by video encoder 255 are then substituted for the frames occurring within the national video feed by processing block 1335. During the generation of the ad insertion frames, decision block 1340 is executing to determine the instant to return programming to the national video feed. The switch occurs as invoked by processing block 1350. Once the switch back to the national video feed has occurred, processing by blocks 1345 and 1355 are effected so that the system interface controller 110 and

channel interface controllers 130, 131, ..., 132 are prepared for the next break, that is, re-initialized by clearing all memories and re-setting the processors to the state of awaiting the next pre-roll cue tone.

Continuing with flow diagram 1400 of FIG. 14, which depicts the processing for the audio portion of the ad insertion signal (audio block 1245 of FIG. 12 couples to audio block 1405 of Fig. 14), decision block 1410 is invoked to determine the instant at which a switch-to-ad signal is to be effected. As depicted by processing block 1415, upon a switch-to-ad indication, DEMUX 235 transmits the MPEG audio components from their location in storage to MPEG audio encoder 240. Next, the synchronized audio produced by audio encoder 240 are then substituted for the audio in the national video feed by processing block 1420. During the generation of the ad insertion of audio, decision block 1425 is executing to determine the instant to return programming to the national video feed. The switch occurs as invoked by processing block 1435. Once the switch back to the national video feed has occurred, processing by blocks 1430 and 1440 are effected so that the system interface controller 110 and channel interface controllers 130, 131, ..., 132 are prepared for the next break, that is, re-initialized by clearing all memories and re-setting the processors to the state of awaiting the next pre-roll cue tone.

System Interface Controller Processing

Now with reference to diagram 1500 of FIG. 15, there is shown in FIG. 15 the interaction of the software tasks executed in transfer processor 215 with certain circuitry of system interface controller 110 and channel interface controllers 130, 131, ..., 132; FIG. 15 elaborates on FIG. 10. In particular, a system with eight channel interface controllers 130, 131, ..., 132 is shown as being serviced by three tasks 1040, 1045, and 1510 executing within transfer processor 215. MPEG-2 transports streams, as identified by cue tone information, are transmitted from signal source 150 over bus 101-1, and are received and stored, via interface bus 206, in the appropriate buffer of memory 220 assigned to corresponding channel interface controller; SCSI task 1040 controls the transport stream flow over bus 101-1 in conjunction with a companion SCSI task 1025 in signal source 150 (FIG. 10). The plurality of interface controllers 130, 131, ..., 132 is shown as operating in conjunction with single compressed data bus task 1045 so that a single system interface controller handles all channel interface controllers. Task 1045 has the major function of transmitting the stored MPEG-2 transport streams via compressed data bus 211 to the each selected one of the channel controllers 130, 131, ..., 132. STATUS lead 515 of compressed data bus 211 is used for supplying the back-flow control bit from each controller (in the assigned slot of sixteen slots for an eight-channel

interface controller system) to inhibit transfer processor from sending MPEG-2 transport streams for channel interface controller which, temporarily, cannot store any more digital data. MPEG-2 transport streams are sequentially retrieved from the appropriate buffers in memory 220, via interface bus 206, under control of compressed data bus task 1045, and delivered sequentially to the selected ones of the channel interface controllers. Loop 1503 associated with task 1045 indicates a process of continuously sending MPEG-2 transport streams to the channel interface controllers as long as back-flow control has not been asserted, or to only selected ones of the channel interface controllers that are free to accept incoming digital data. Transfer processor 215 and system processor 225 can communicate via inter-processor task 1510 which can operate on memory 220; loop 1505 indicates that inter-processor task 1510 in continuously operational.

Now with reference to diagram 1600 of FIG. 16, there is shown in FIG. 16 the interaction of the software tasks executed in system processor 225 with the certain circuitry of system interface controller 110 and channel interface controllers 130, 131, ..., 132; FIG. 16 elaborates on FIG. 10. In particular, a system with eight channel interface controllers 130, 131, ..., 132 is shown as being serviced by four tasks 1015, 1020, 1025, and 1510 executing within system processor 225. Task 1020 has the major function of monitoring STATUS lead 515 for the interrupt

bits in eight alternating ones of the sixteen slots, and to act upon any asserted interrupt bit by informing control bus task 1015, via task path 1603, of the need to service the identified ones of the channel interface controllers over control bus 212. As priorly discussed, the receipt of a pre-roll cue tone will trigger such response. Control bus task 1015 and Ethernet task 1025 interact, as indicated by task path 1609, so that information obtained off control bus 212 and destined for signal source 150 can be interchanged over Ethernet link 101-2. System processor 225 and transfer processor 215 can communicate via inter-processor task 1610 which can operate on memory 220; loop 1605 indicates that inter-processor task 1610 in continuously operational.

Channel Interface Controller Processing

Now with reference to diagram 1700 of FIG. 17, there is shown in FIG. 17 the interaction of the software tasks executed in channel processor 265 with the certain circuitry of each channel interface controller 130, 131, ..., or 132; FIG. 17 elaborates on FIG. 10. In particular, one of a plurality of channel interface controllers 130, 131, ..., 132 (say 130) is shown along with five tasks 1005, 1010, 1050, 1710, and 1720 executing within channel processor 265. Cue tone task 1005 processes each incoming pre-roll cue tone to: (i) inform control bus task 1010 of the need to validate incoming cue tone information, insert an interrupt in STATUS lead 515 to pass along valid cue tone

information to compressed data bus task 1050, and store the cue tone information in dual-port RAM 267 (FIG. 9); (ii) activate decode task 1520, which includes activating the count-time clock; and (iii) activate monitor task 1510 to initiate monitoring of the video and/or audio memories in DEMUX 235 to determine when the video and/or audio memories can no longer accept incoming MPEG-2 transport streams. The dashed lines in FIG. 17 depict that each task, through software, can interact with the hardware component pointed to by each dashed line. For instance, dashed line 1701 indicates that monitor task 1510 can monitor the "fill" level of the video memory -- typically this is accomplished through the software mechanism of monitoring an address pointer to the last area in memory used to store an incoming MPEG elementary stream parsed from an incoming MPEG-2 transport stream. For example, dashed lines 1708 and 1709, respectively, indicate that compressed data bus task 1050 controls the reception of the incoming MPEG-2 transport streams, based on header information that a stream is either a video or audio stream, to either the video memory or audio memory of DEMUX 235. Decode task 1520 initializes all decoding parameters in MPEG video decoder 250 and MPEG audio encoder 240, as depicted by dashed lines 1703 and 1704; also, under control of the count-down clock, initiates activation of switch 1730 (which is a high-level circuitry block encompassing both video switch 260 and audio switch 245 of FIG. 2), as depicted by dashed line 1707, to thereby substitute the MPEG-2 derived signal into the

national feed programming for a break interval, and then switch back to the national feed programming upon the completion of the break interval.

CLAIMS

We claim:

1. A system for delivering an output signal corresponding to a primary source in one interval and representative of an autonomous signal source in another interval, wherein the primary source includes: a primary signal; and a control signal indicative of said another interval, the primary source being derived from a national network television feed signal so that the primary signal is a television signal having a given composite synchronization signal, and wherein the autonomous signal source includes stored data, the system comprising:

(a) a signal generator, responsive to the primary signal, for generating a timing signal from the primary signal, said signal generator including

(i) a detector for detecting the composite synchronization signal in the national feed television signal, wherein said timing signal is generated in correspondence to the detected composite synchronization signal;

(b) a converter, coupled to the autonomous signal source, for converting a data stream transmitted by the autonomous signal source to a secondary signal synchronized to the timing signal, said data stream selected from the stored data in response to the control signal;

(c) a flow regulator, coupled to the autonomous signal source and responsive to said converter, for controlling the flow of said data stream transmitted from the autonomous signal source to said converter; and

(d) a transmitter, responsive to the primary signal and the secondary signal, for transmitting the primary signal during said one interval as the output signal, and the secondary signal as the output signal during said another interval in response to the control signal.

2. The system as recited in claim 1 wherein the composite synchronization signal is composed of a vertical synchronization signal and a horizontal synchronization signal, wherein said detector includes a stripper for stripping the vertical synchronization signal and horizontal synchronization signal from the national feed television signal, and wherein said signal generator includes a genlock circuit, responsive to the horizontal synchronization signal, and a logic circuit, responsive to the vertical synchronization signal and the horizontal synchronization signal, said genlock circuit and said logic circuit arranged to cooperatively generate said timing signal with a frequency and a phase corresponding to the composite synchronization signal.

3. The system as recited in claim 1 wherein the composite synchronization signal is composed of a vertical synchronization signal and a horizontal synchronization signal, wherein said detector includes a stripper for stripping the vertical synchronization signal and horizontal synchronization signal from the national feed television signal, and wherein said signal generator includes

a phase detector circuit, responsive to said stripper, to produce a phase-detected signal from the horizontal synchronization signal,

a voltage controlled oscillator circuit, responsive to said phase-detected signal, to produce a voltage controlled signal,

a phase-locked loop circuit, responsive to said voltage controlled signal, to produce a phase-locked signal, and

a logic circuit, responsive to said phase-locked loop circuit and said stripper, for processing said phase-locked loop signal and the vertical synchronization signal

to produce said timing signal, a regenerated horizontal output from said logic circuit being fed-back as another input to said phase detector circuit so that said phase-detected signal controls a frequency and phase of said voltage controlled oscillator circuit to thereby generate said timing signal with a frequency and a phase corresponding to the given composite synchronization signal.

4. The system as recited in claim 3 wherein said logic circuit produces a regenerated vertical synchronization signal corresponding to the vertical synchronization signal, and said transmitter switches from the primary signal to the secondary signal in correspondence to the regenerated vertical synchronization signal.

5. A system for delivering an output signal corresponding to a primary source in one interval and representative of an autonomous signal source in another interval, wherein the primary source includes: a primary signal; and a control signal indicative of said another interval, the primary source being derived from a national network television feed signal so that the primary signal is a television signal having a given composite synchronization signal, and wherein the autonomous signal source includes stored data, the system comprising:

(a) a signal generator, responsive to the primary source, for generating a timing signal from the primary signal, said signal generator including

(i) a detector for detecting the composite synchronization signal in the national feed television signal, wherein said timing signal is generated in correspondence to the detected composite synchronization signal;

(b) a storage device, coupled to the secondary source, for storing a data stream communicated by the

secondary source and selected with reference to the control signal;

(c) a converter, coupled to said storage device, for converting the stored data stream to a secondary signal synchronized to the timing signal;

(d) means, coupled to the secondary source and the storage device, for controlling the flow of said data stream; and

(e) a switch, responsive to the primary signal and the secondary signal, for switching from the primary signal to the secondary signal in response to the control signal.

6. The system as recited in claim 5 wherein the composite synchronization signal is composed of a vertical synchronization signal and a horizontal synchronization signal, wherein said detector includes a stripper for stripping the vertical synchronization signal and horizontal synchronization signal from the national feed television signal, and wherein said signal generator includes a genlock circuit, responsive to the horizontal synchronization signal, and a logic circuit, responsive to the vertical synchronization signal and the horizontal synchronization signal, said genlock circuit and said logic circuit arranged to cooperatively generate said timing signal with a frequency and a phase corresponding to the composite synchronization signal.

7. The system as recited in claim 5 wherein the composite synchronization signal is composed of a vertical synchronization signal and a horizontal synchronization signal, wherein said detector includes a stripper for stripping the vertical synchronization signal and horizontal synchronization signal from the national feed television signal, and wherein said signal generator includes

a phase detector circuit responsive to said stripper to produce a phase-detected signal from the horizontal synchronization signal,

a voltage controlled oscillator circuit responsive to said phase-detected signal to produce a voltage controlled signal,

a phase-locked loop circuit responsive to said voltage controlled signal to produce a phase-locked signal, and

a logic circuit, responsive to said phase-locked loop circuit and said stripper, for processing said phase-locked loop signal and the vertical synchronization signal to produce said timing signal, a regenerated horizontal output from said logic circuit being fed-back as another input to said phase detector circuit so that said phase-detected signal controls a frequency and phase of said voltage controlled oscillator circuit to thereby generate said timing signal with a frequency and a phase corresponding to the given composite synchronization signal.

8. The system as recited in claim 7 wherein said logic circuit produces a regenerated vertical synchronization signal corresponding to the vertical synchronization signal, and said transmitter switches from the primary signal to the secondary signal in correspondence to the regenerated vertical synchronization signal.

9. A signal processor for generating an output signal alternately produced from either a video source or an autonomous signal source, wherein the video source includes: a television signal; and a cue tone indicating an interval for which the output signal corresponds to the autonomous signal source, the television signal including a composite synchronization signal, and wherein the autonomous signal source includes stored data, the signal processor comprising

a channel interface controller, coupled to the video source, for emitting the output signal, and

a system interface controller, coupled to the autonomous signal source and said channel interface controller, for storing a data stream provided by the autonomous signal source as stored data,

said channel interface controller including

a signal generator for generating a timing signal from the television signal, said signal generator including

a detector for detecting the composite synchronization signal in the television signal, and

a unit, responsive to said detector, for producing said timing signal in correspondence to the composite synchronization signal,

a transmitter for transmitting the stored data from said system interface controller,

a converter for converting the stored data to an alternative television signal synchronized to the timing signal, and

a switch for switching between the television signal and the alternative television signal in correspondence to the cue tone,

wherein said system interface controller includes a flow regulator for controlling the flow of said data stream in response to said transmitter.

10. The system as recited in claim 9 wherein the composite synchronization signal is composed of a vertical synchronization signal and a horizontal synchronization signal, wherein said detector includes a stripper for stripping the vertical synchronization signal and horizontal synchronization signal from the television signal, and wherein said unit includes a genlock circuit, responsive to the horizontal synchronization signal, and a logic circuit,

responsive to the vertical synchronization signal and the horizontal synchronization signal, said genlock circuit and said logic circuit arranged to cooperatively generate said timing signal with a frequency and a phase corresponding to the composite synchronization signal.

11. The system as recited in claim 10 wherein the composite synchronization signal is composed of a vertical synchronization signal and a horizontal synchronization signal, wherein said detector includes a stripper for stripping the vertical synchronization signal and horizontal synchronization signal from the television signal, and wherein said unit includes

a phase detector circuit, responsive to said stripper, to produce a phase-detected signal from the horizontal synchronization signal,

a voltage controlled oscillator circuit, responsive to said phase-detected signal, to produce a voltage controlled signal,

a phase-locked loop circuit, responsive to said voltage controlled signal, to produce a phase-locked signal, and

a logic circuit, responsive to said phase-locked loop circuit and said stripper, for processing said phase-locked loop signal and the vertical synchronization signal to produce said timing signal, a regenerated horizontal output from said logic circuit being fed-back as another input to said phase detector circuit so that said phase-detected signal controls a frequency and phase of said voltage controlled oscillator circuit to thereby generate said timing signal with a frequency and a phase corresponding to the given composite synchronization signal.

12. The system as recited in claim 11 wherein said logic circuit produces a regenerated vertical synchronization

signal corresponding to the vertical synchronization signal, and said transmitter switches from the primary signal to the secondary signal in correspondence to the regenerated vertical synchronization signal.

13. A signal processor for generating a plurality of output signals, each of the output signals alternately produced from either an autonomous signal source or a corresponding one of a plurality of video sources, wherein each of the video sources includes: a television signal; and a cue tone indicating an interval for which one of the output signals corresponds to the autonomous signal source, the television signal including a composite synchronization signal, and wherein the autonomous signal source includes stored data, the signal processor comprising

a plurality of channel interface controllers, coupled to the video sources, for emitting each of the output signals from a corresponding one of the video sources, and

a system interface controller, coupled to the autonomous signal source and said channel interface controllers, for receiving a data stream communicated by the autonomous signal source, and for storing a plurality of substreams of said data stream as a plurality of stored data corresponding to each of said channel interface controllers, said data stream being formed in response to each cue tone,

each of said channel interface controllers including

(a) a selector for choosing one of the video sources to thereby determine a selected video source and, correspondingly, a selected television signal and a selected cue tone;

(b) a signal generator for generating a timing signal from said selected television signal to produce a selected timing signal, said signal generator

including

a detector for detecting the composite synchronization signal in the television signal, wherein said timing signal is generated in correspondence to the detected composite synchronization signal;

(c) a transmitter for transmitting one of the plurality of the stored data from said system interface controller in correspondence to the selected cue tone to determine selected stored data,

(d) a converter for converting the selected stored data to an alternative television signal synchronized to the selected timing signal, said converter operating at a given rate of conversion; and

(e) a switch for switching between the selected television signal and the alternative television signal in correspondence to the selected cue tone, and

said system interface controller including a flow regulator for controlling the flow of the data stream based on each said rate of conversion.

14. The system as recited in claim 13 wherein the composite synchronization signal is composed of a vertical synchronization signal and a horizontal synchronization signal, wherein said detector includes means for stripping the vertical synchronization signal and horizontal synchronization signal from the television signal, and wherein said signal generator includes a genlock circuit, responsive to the horizontal synchronization signal, and a logic circuit, responsive to the vertical synchronization signal and the horizontal synchronization signal, said genlock circuit and said logic circuit arranged to cooperatively generate said timing signal with a frequency and a phase corresponding to the composite synchronization signal.

15. The system as recited in claim 13 wherein the composite synchronization signal is composed of a vertical synchronization signal and a horizontal synchronization signal, wherein said detector includes a stripper for stripping the vertical synchronization signal and horizontal synchronization signal from the national feed television signal, and wherein said signal generator includes

a phase detector circuit, responsive to said stripper, to produce a phase-detected signal from the horizontal synchronization signal,

a voltage controlled oscillator circuit, responsive to said phase-detected signal, to produce a voltage controlled signal,

a phase-locked loop circuit, responsive to said voltage controlled signal, to produce a phase-locked signal, and

a logic circuit, responsive to said phase-locked loop circuit and said stripper, for processing said phase-locked loop signal and the vertical synchronization signal to produce said timing signal, a regenerated horizontal output from said logic circuit being fed-back as another input to said phase detector circuit so that said phase-detected signal controls a frequency and phase of said voltage controlled oscillator circuit to thereby generate said timing signal with a frequency and a phase corresponding to the given composite synchronization signal.

16. The system as recited in claim 15 wherein said logic circuit produces a regenerated vertical synchronization signal corresponding to the vertical synchronization signal, and said transmitter switches from the primary signal to the secondary signal in correspondence to the regenerated vertical synchronization signal.

17. A method for delivering an output signal corresponding to a primary source in one interval and representative of an autonomous signal source in another interval, wherein the primary source includes: a primary signal; and a control signal indicative of said another interval, the primary source being derived from a national network television feed signal so that the primary signal is a television signal having a given composite synchronization signal, and wherein the autonomous signal source includes stored data, the method comprising the steps of:

(a) generating a timing signal from the primary signal, said step of generating including the sub-steps of

(i) detecting the composite synchronization signal in the national television feed signal, and

(ii) producing said timing signal in correspondence to the composite synchronization signal;

(b) selecting data from the stored data in response to the control signal to produce a data stream;

(c) transmitting said data stream from the autonomous signal source;

(d) converting said data stream to a secondary signal synchronized to the timing signal;

(e) controlling the flow of said data stream transmitted from the autonomous signal source; and

(f) transmitting the primary signal during said one interval as the output signal, and the secondary signal as the output signal during said another interval in response to the control signal.

18. The method as recited in claim 17 wherein said sub-step of detecting includes the step of stripping the vertical synchronization signal and horizontal synchronization signal from the national feed television signal, and wherein said sub-step of producing includes the step of generating said timing signal with a frequency and a phase corresponding to the composite synchronization signal.

19. The method as recited in claim 17 wherein said sub-step of detecting includes the step of stripping the vertical synchronization signal and horizontal synchronization signal from the national feed television signal, and wherein said sub-step of producing includes steps of

processing the horizontal synchronization signal with a phase detector circuit to produce a phase-detected signal from the horizontal synchronization signal,

processing said phase-detected signal with a voltage controlled oscillator circuit to produce a voltage controlled signal,

processing said voltage controlled signal with a phase-locked loop circuit to produce a phase-locked signal, and

processing said phase-locked loop signal and the vertical synchronization signal with a logic circuit to produce said timing signal, said step of processing said phase-locked loop signal including the step of feeding-back a regenerated horizontal synchronization signal from said logic circuit as another input to said phase detector circuit so that said phase-detected signal controls a frequency and phase of said voltage controlled oscillator circuit to thereby generate said timing signal with a frequency and a phase corresponding to the composite synchronization signal.

20. The method as recited in claim 19 wherein said logic circuit produces a regenerated vertical synchronization signal corresponding to the vertical synchronization signal, and said step of transmitting includes the step of switching from the primary signal to the secondary signal in correspondence to the regenerated vertical synchronization signal.

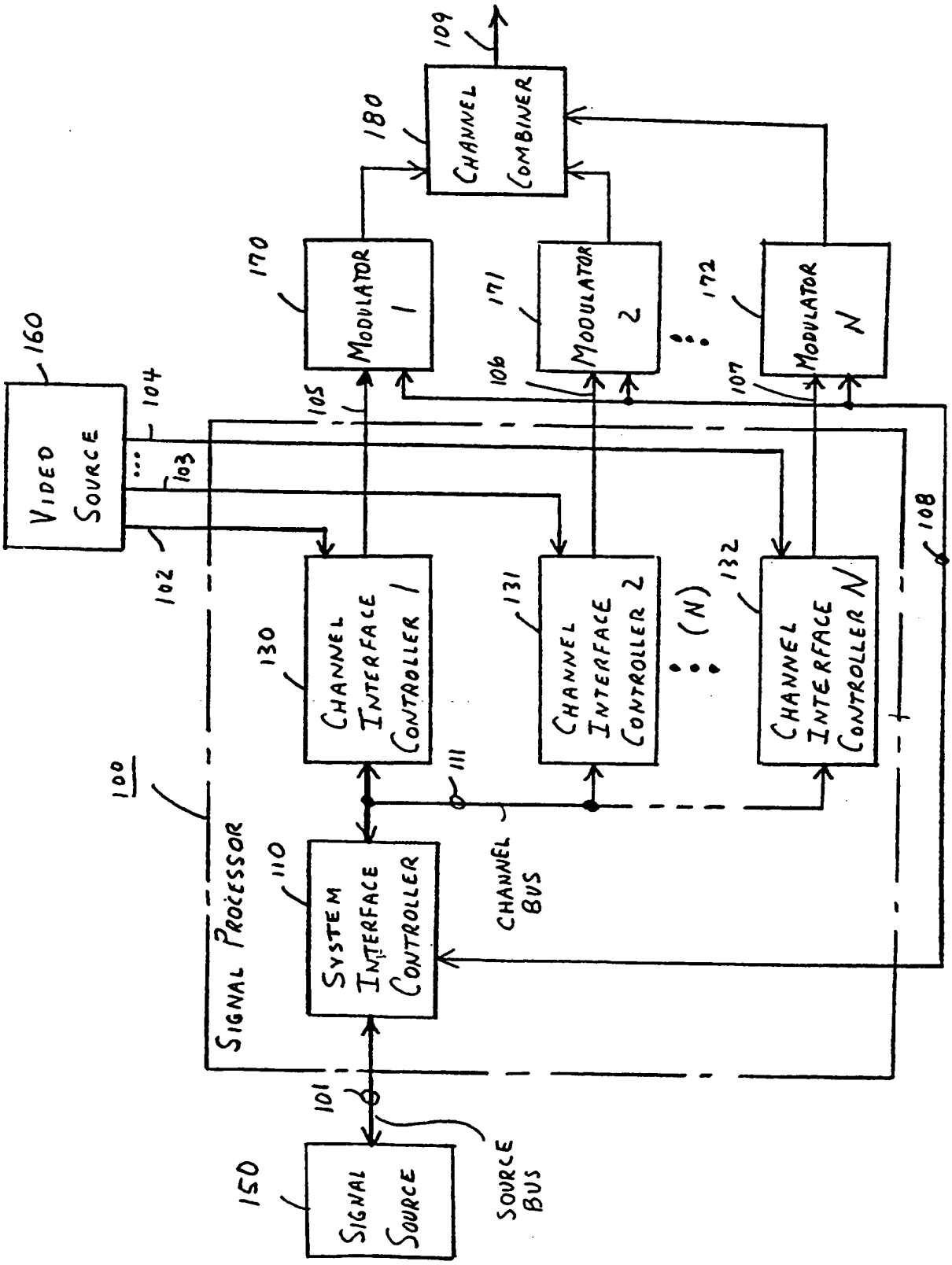

FIG. 1

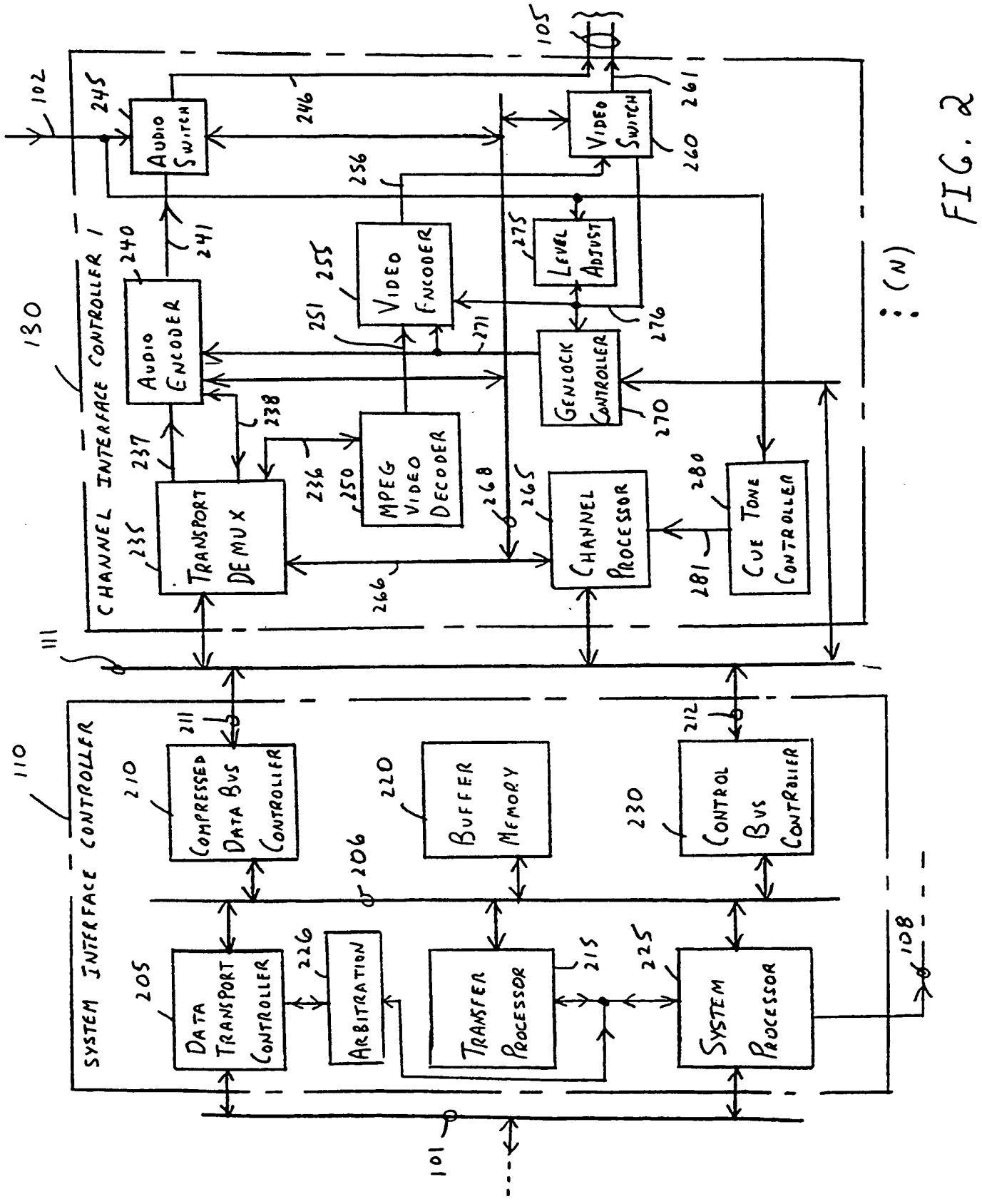

FIG. 2

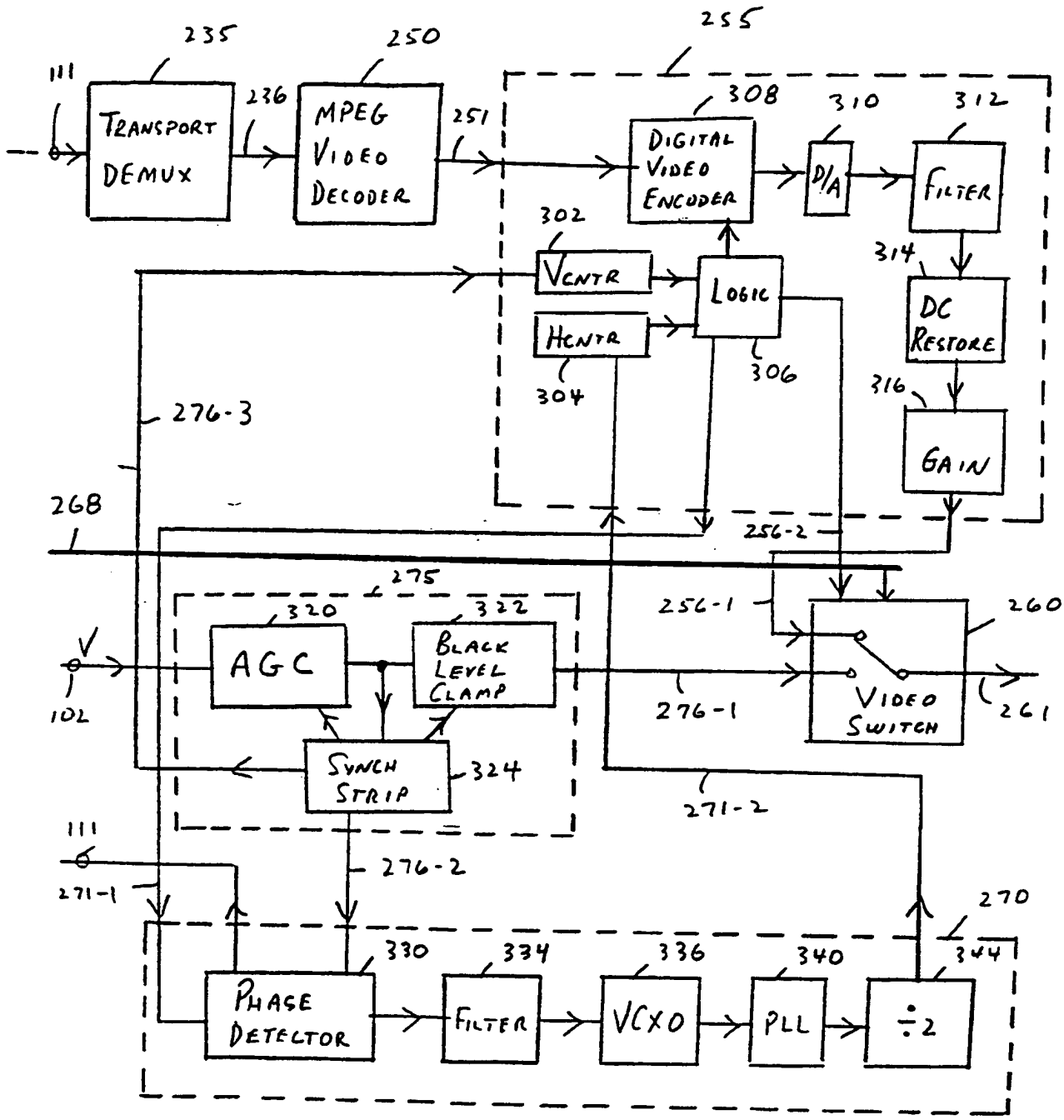

FIG. 3

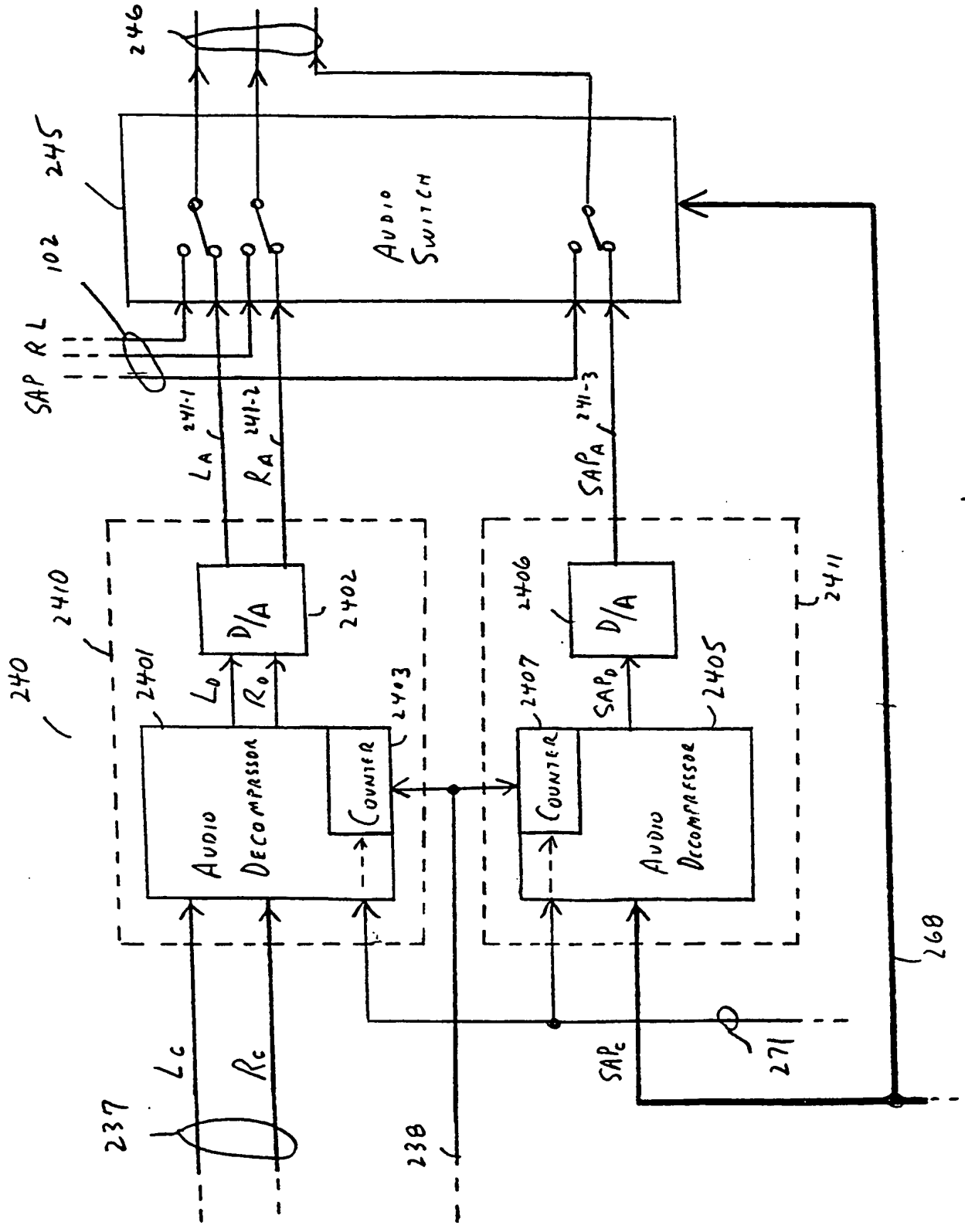

FIG. 4

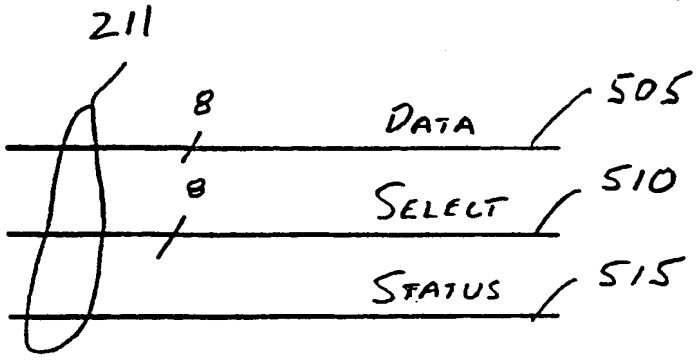

FIG. 5

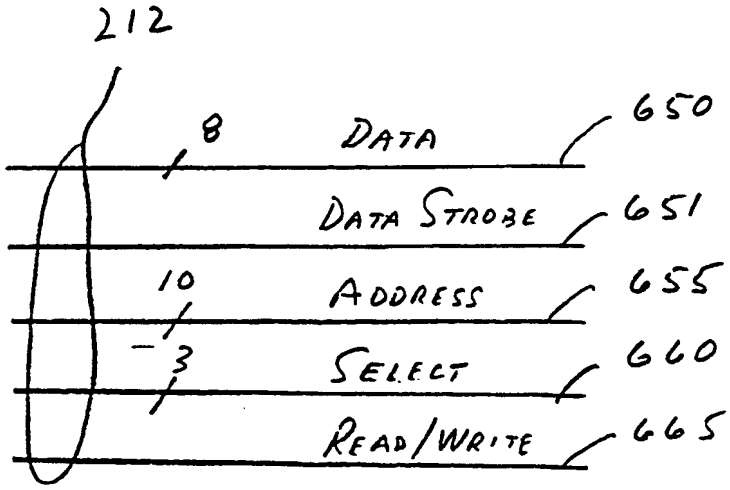

FIG. 6

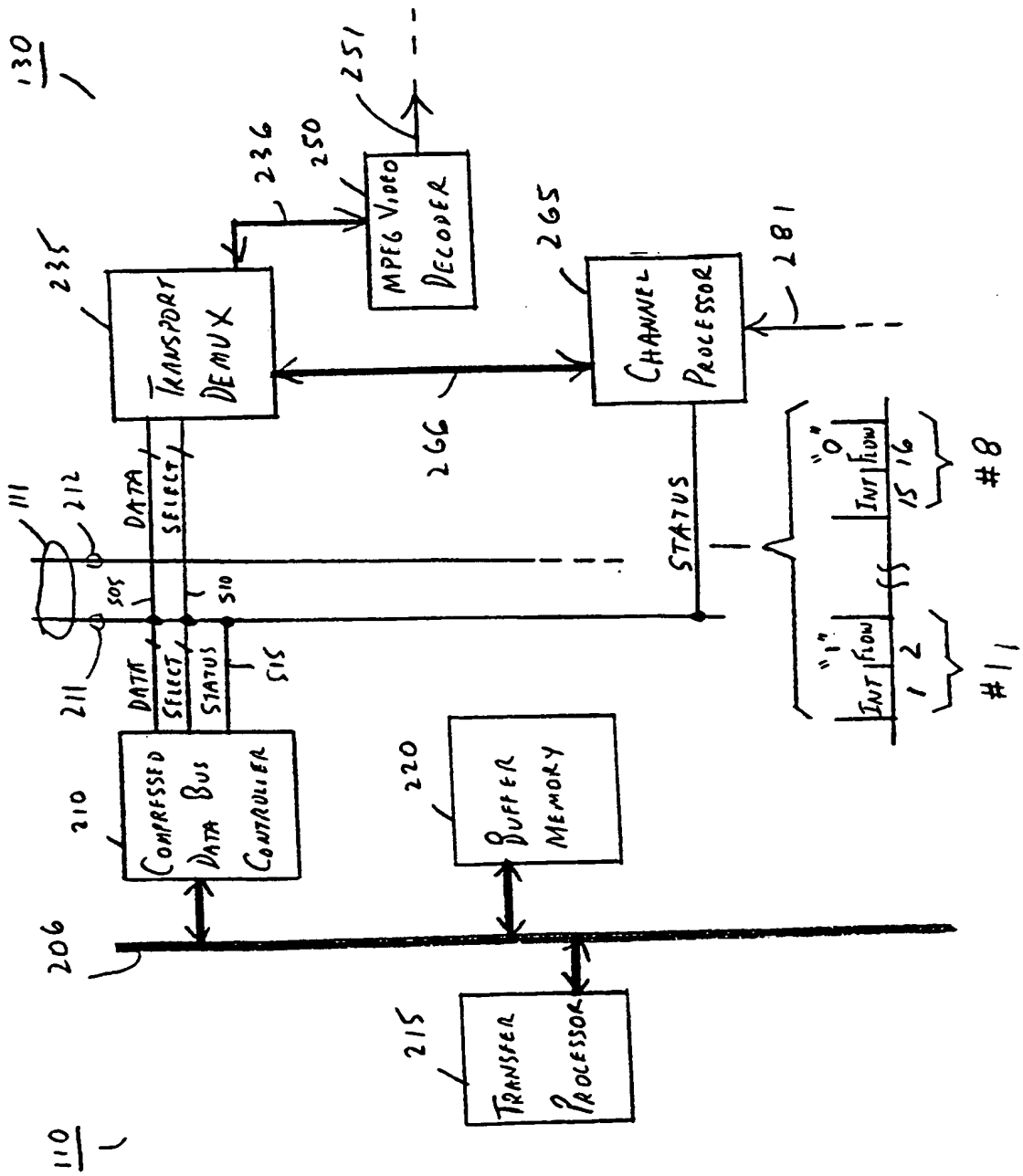

FIG. 7

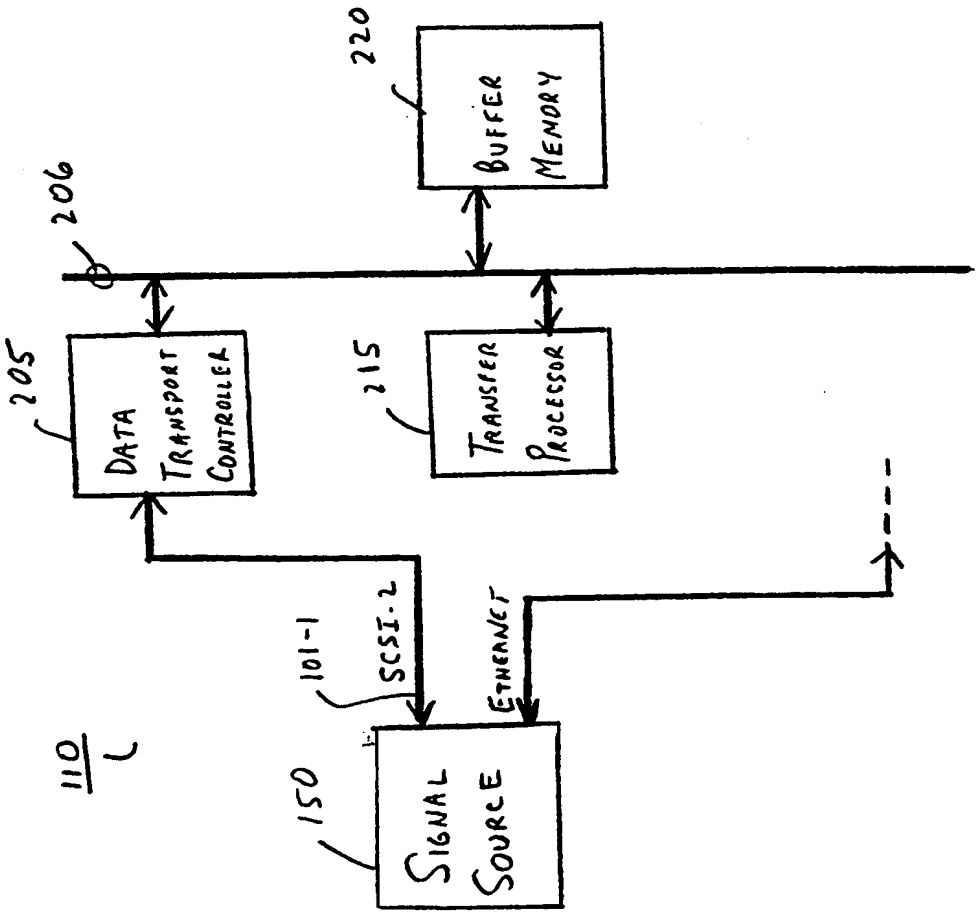

FIG. 8

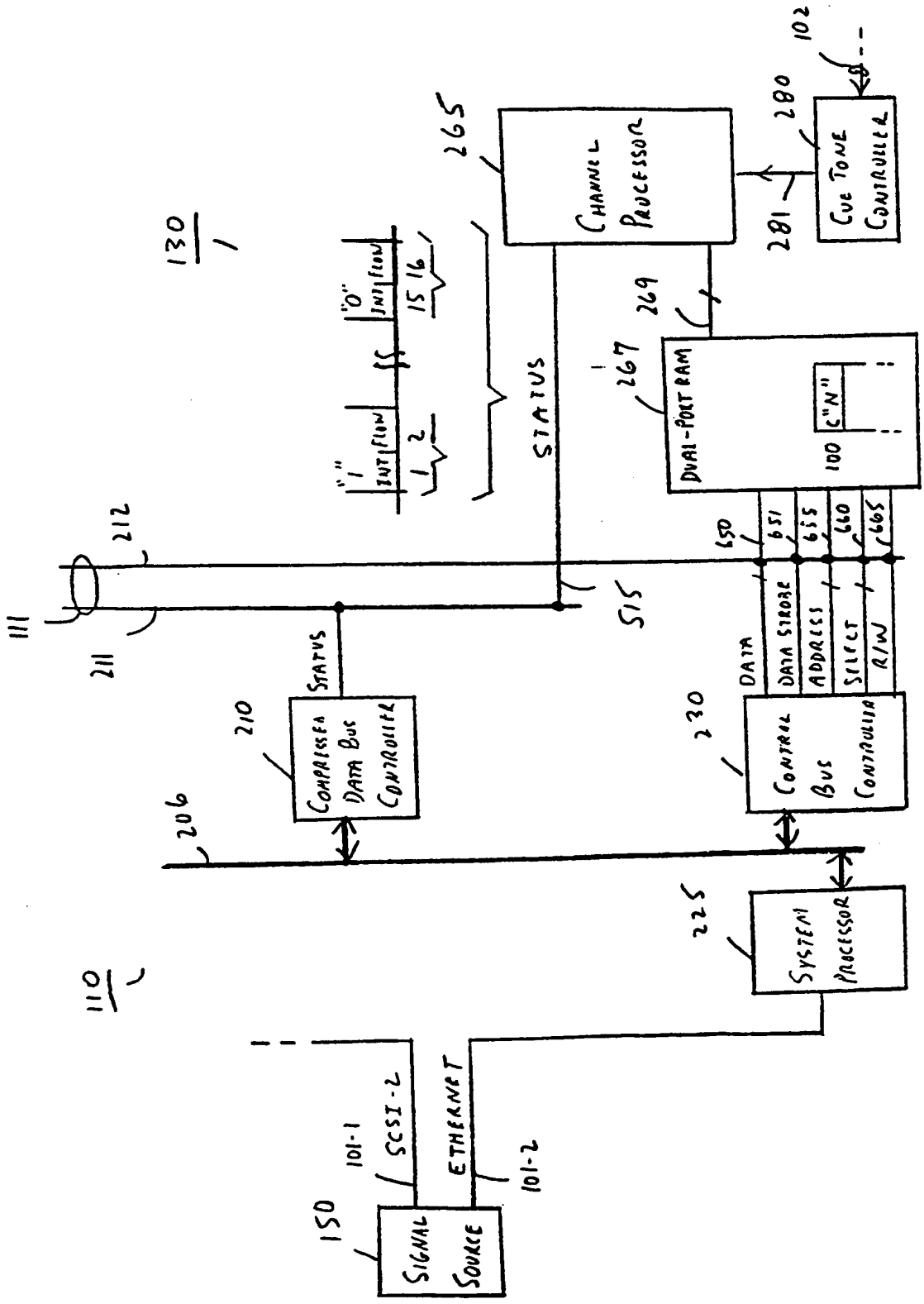

FIG. 9

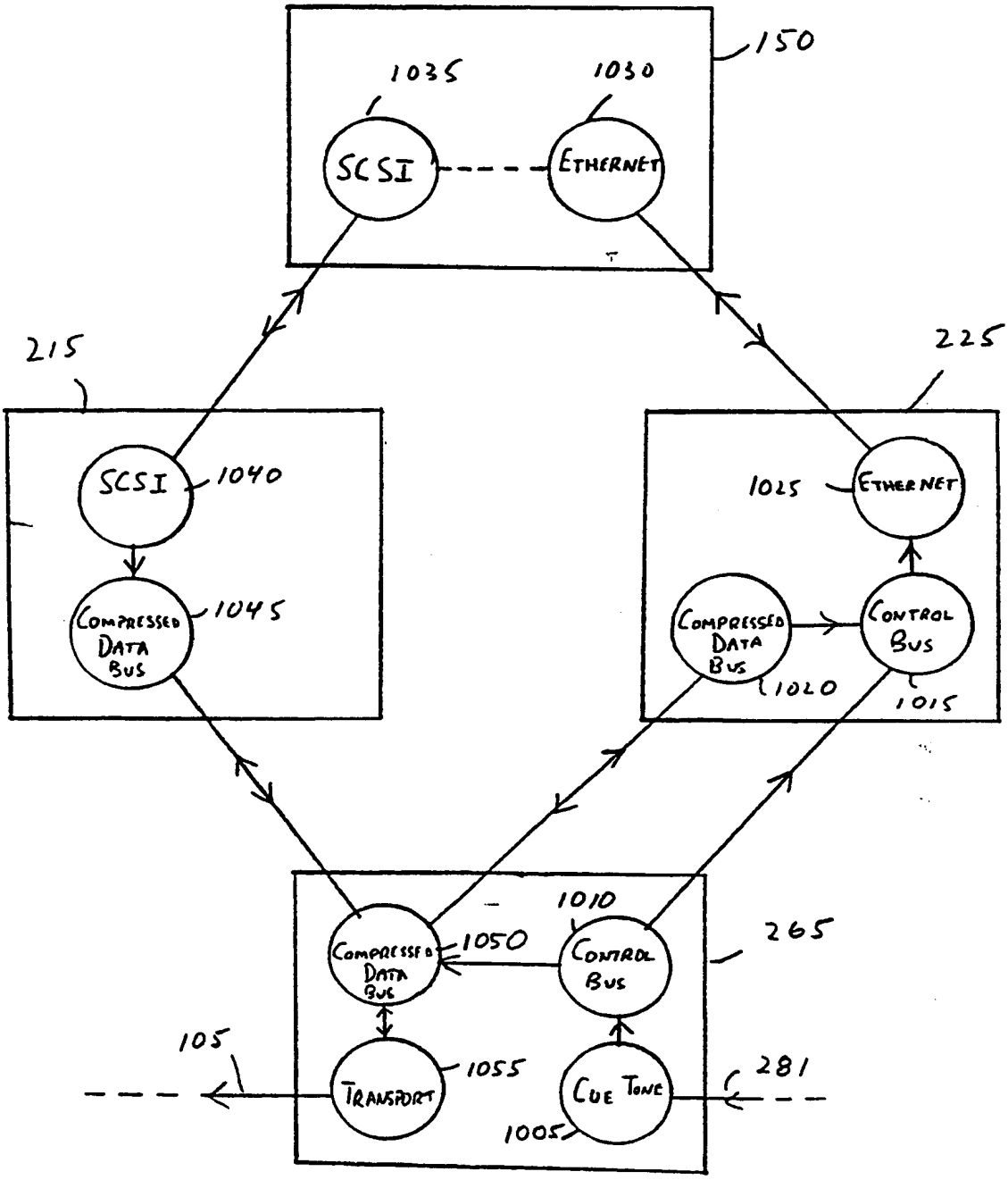

FIG. 10

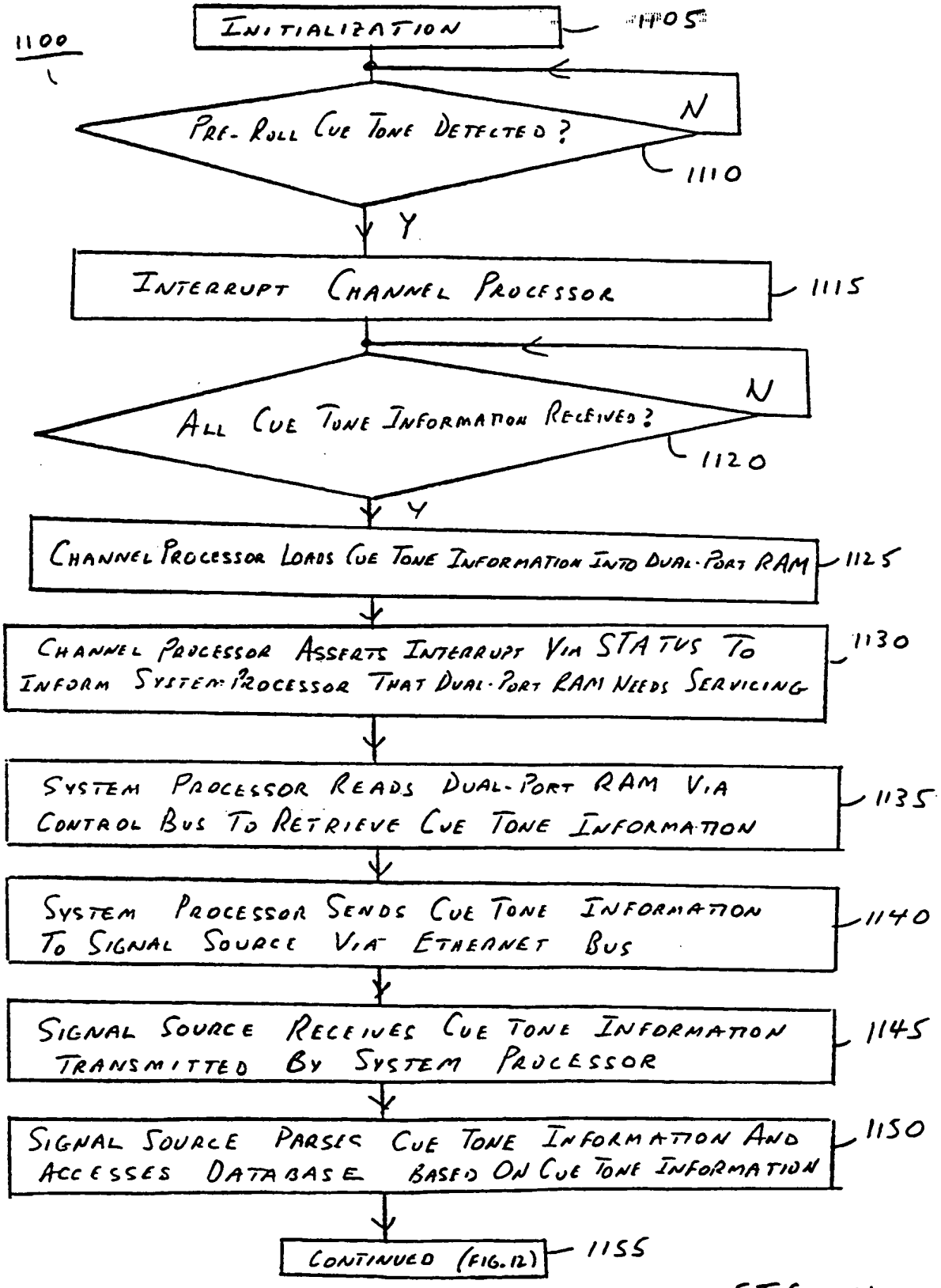

FIG. 11

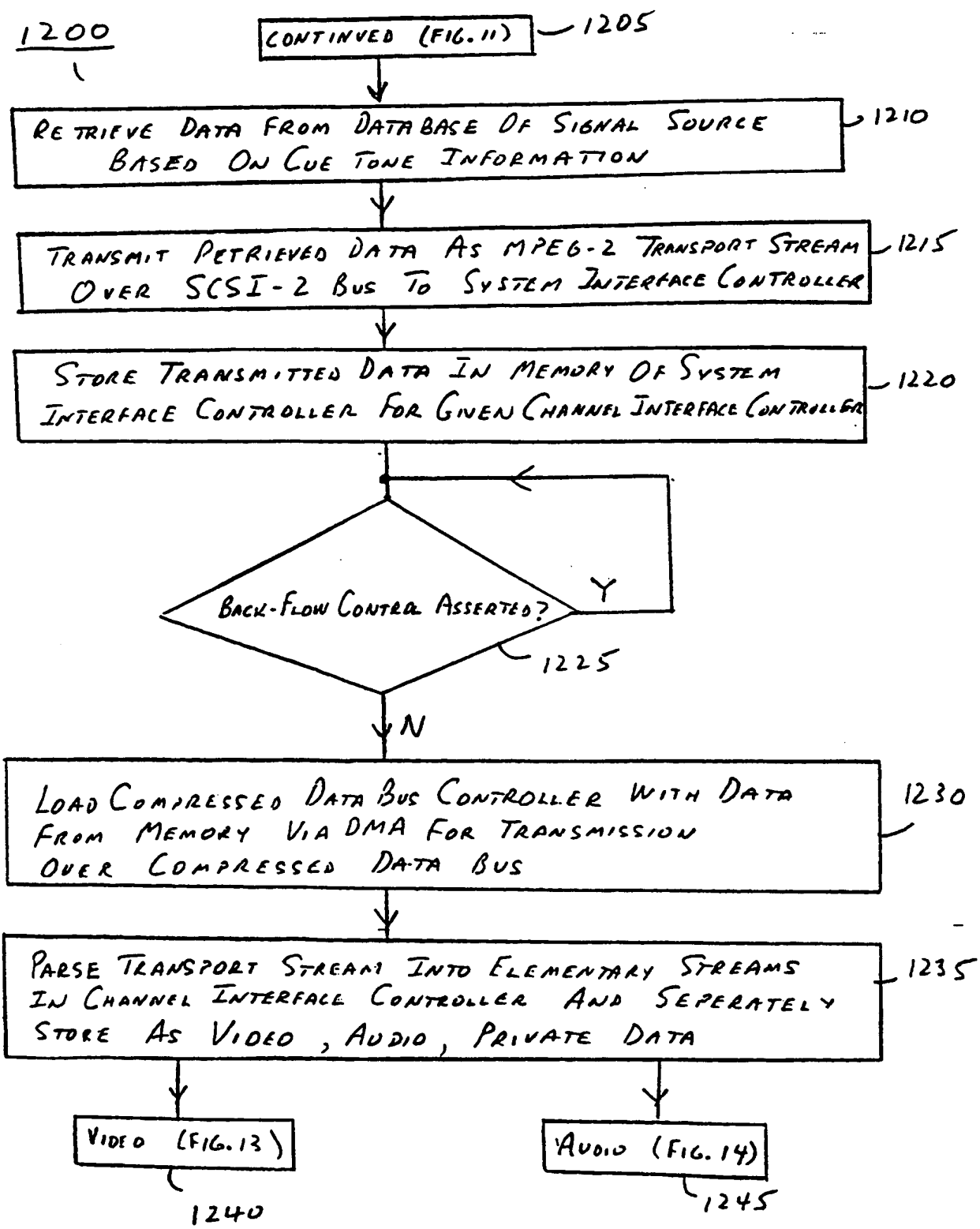

FIG. 12

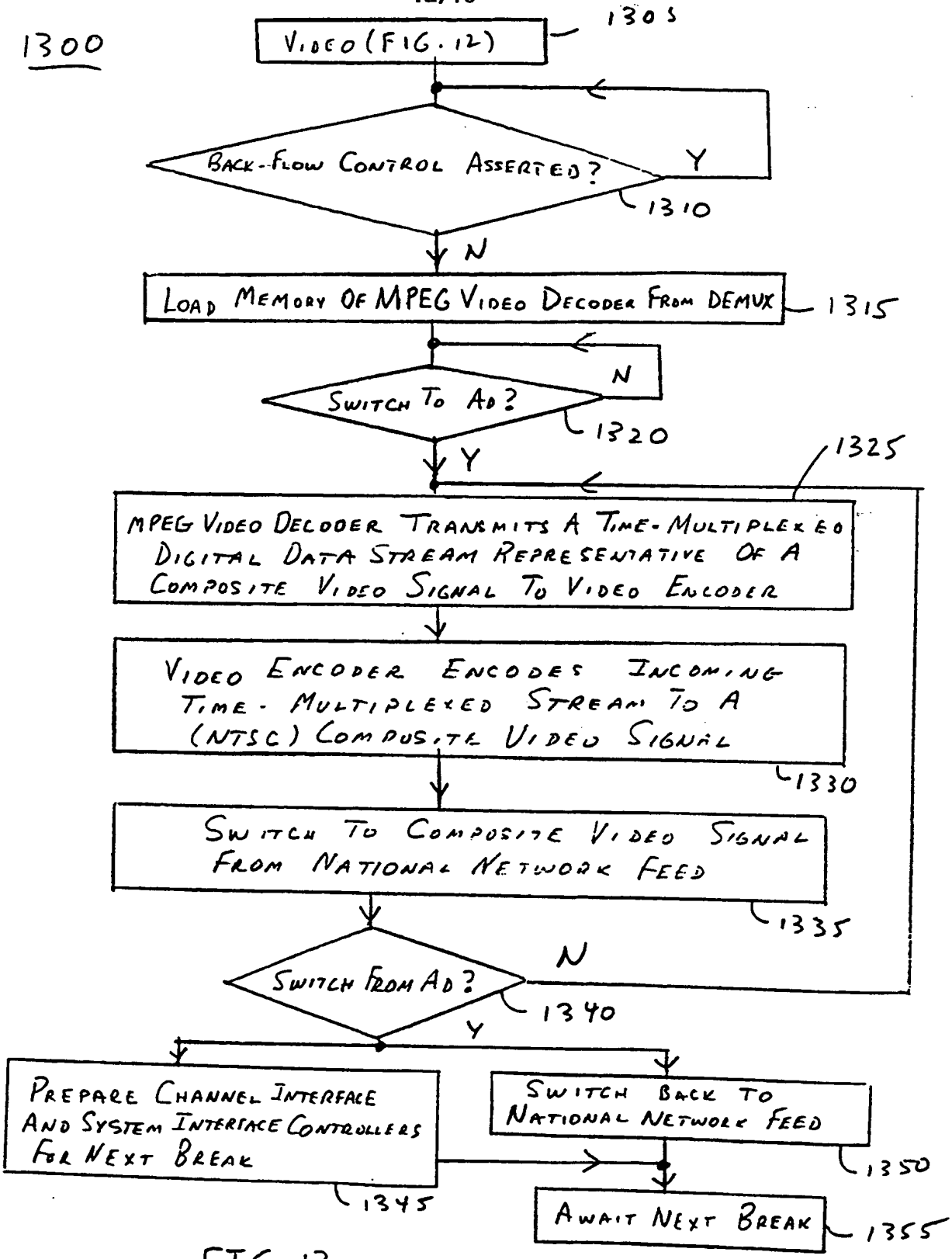

FIG. 13

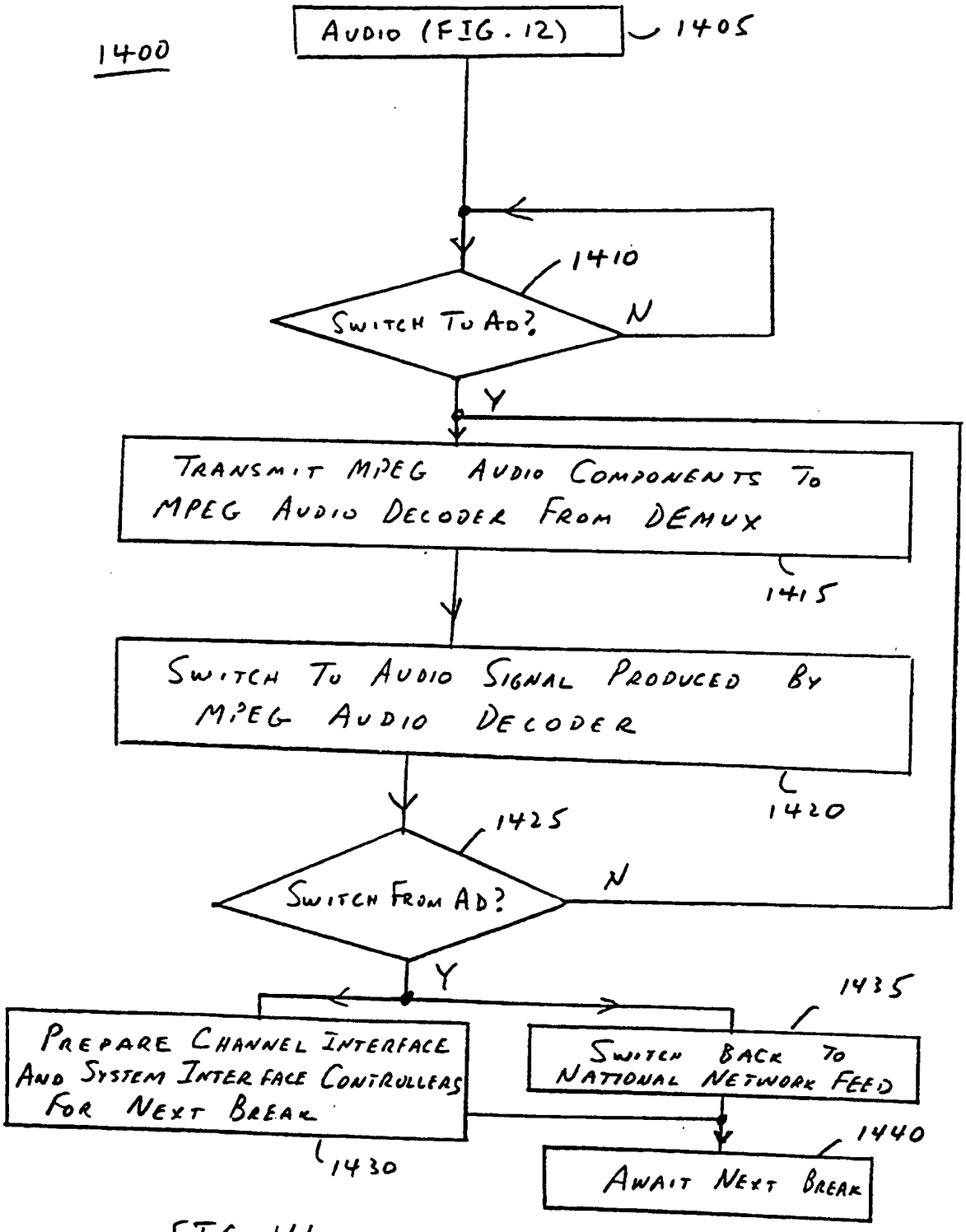

FIG. 14

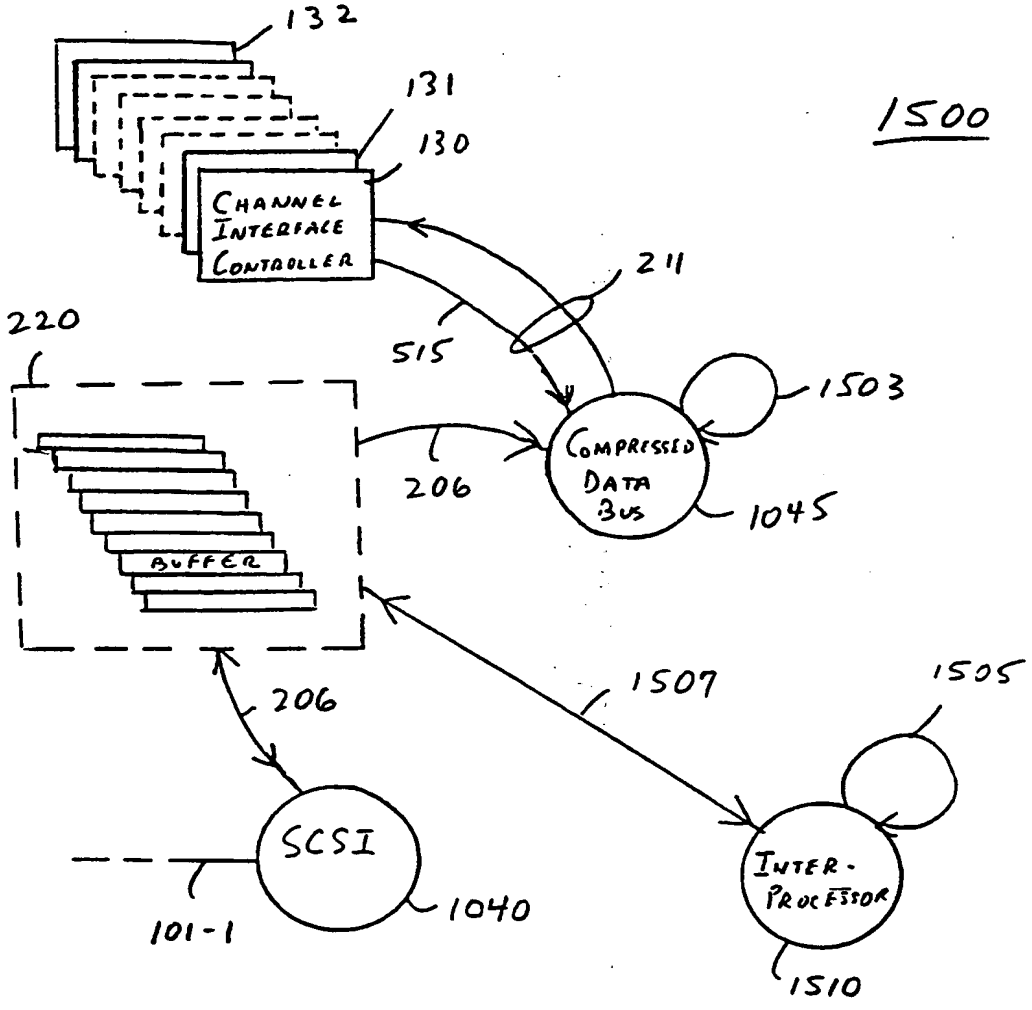

FIG. 15

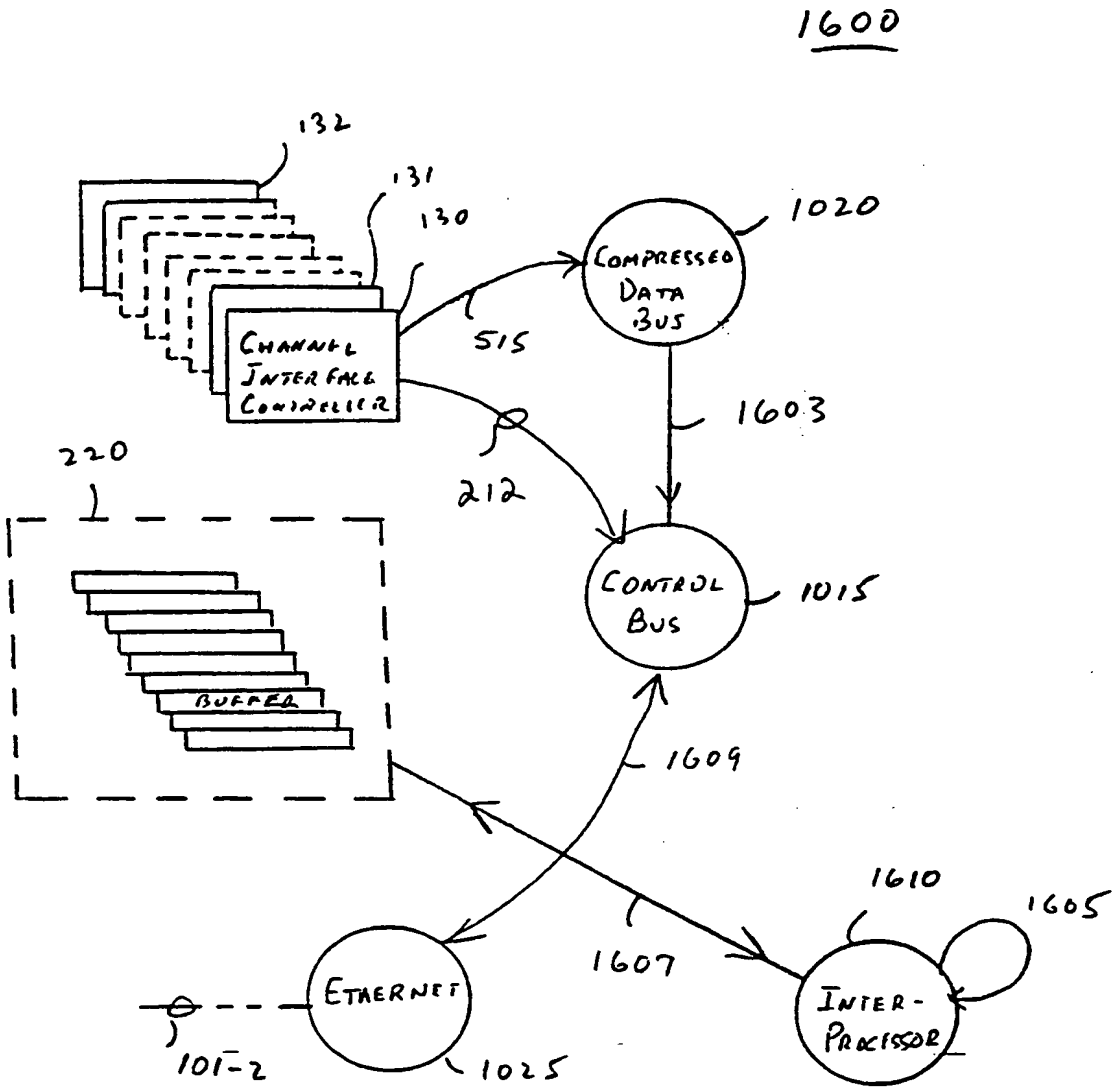

FIG. 16

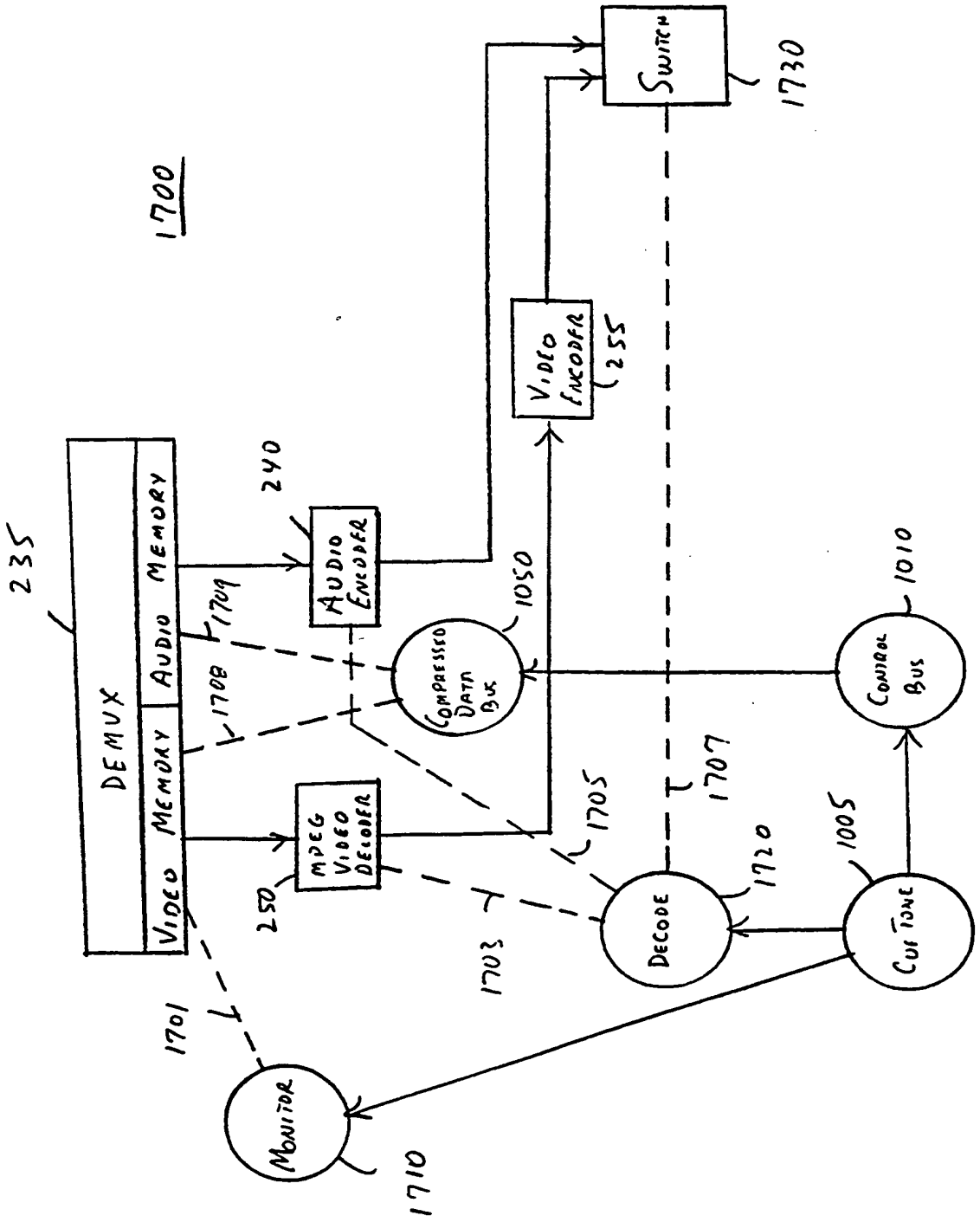

FIG. 17